PCI 9052 Data Book

Version 1.02

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Timing DIagrams

REVISION HISTORY

Date	Revision	Comment
08/16/1997	1.0	Initial release
12/02/1999	1.01	Applied minor format changes and corrected minor typographical errors. Changed title from “Data Sheet” to “Data Book.” Added 800 phone number. Changed copyright date to 1999. Added primary title page, disclaimer and trademarks, part number, and list of Figures, Tables, and Timing Diagrams. Changed “negate” to “de-assert.” Added note to appropriate figures that represent a bus cycle. Changed “field” to “bit” in register-related tables. Table 5-15, PCIBAR3[3], corrected reference to LAS1BRD. Section 7, requenced content, added section headings, and correctly mapped the input and output waveforms with their respective captions. Timing Diagram 9-24, corrected reference to Lword quantity.
02/09/2000	1.02	Fix timing diagrams on pages 69-74 (last signal name was cut off from view).

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PCI 9052

December 1999
VERSION 1.01

PCI Bus TARGET Chip with Glueless ISA Interface Logic for Low Cost Adapters

1. GENERAL DESCRIPTION

The PCI 9052 provides a compact high-performance PCI bus target (slave) interface for adapter boards. The PCI 9052 is designed to connect a wide variety of local bus designs to the PCI bus and allow relatively slow local bus designs to achieve 132 MB/sec burst transfers on the PCI bus.

The PCI 9052 can be programmed to connect directly to multiplexed or non-multiplexed 8-, 16-, or 32-bit local bus. 8- and 16-bit modes enable easy conversion of ISA designs to PCI. (Refer to Figure 1-1.)

The PCI 9052 contains a read and write FIFO to speed match 32-bit wide, 33 MHz PCI bus to a local bus, which may be narrower or slower. Up to five Local Address Spaces and up to four chip selects are supported.

1.1 Major Features

PCI Specification v2.1 compliant. The PCI 9052 is compliant with PCI Specification v2.1, supporting low cost slave adapters. The chip allows simple conversion of ISA adapters to PCI.

Direct slave (Target) data transfer mode. The PCI 9052 supports burst memory-mapped and I/O-mapped accesses from the PCI bus to the local bus. The read and write FIFOs enable high-performance bursting on the local and PCI buses. The PCI bus is always bursting; however, the local bus can be set to bursting or continuous single cycle.

Interrupt generator. The PCI 9052 can generate a PCI interrupt from two local bus interrupt inputs.

Clock. The PCI 9052 local bus interface runs from a local TTL clock and generates necessary internal clocks. This clock runs asynchronously to the PCI clock, allowing the local bus to run at an independent rate from PCI clock. The buffered PCI bus clock (BCLKO) may be connected to the local bus clock (LCLK).

Programmable local bus configurations. The PCI 9052 supports 8-, 1, or 32-bit local buses, which may be multiplexed or non-multiplexed. The PCI 9052 has four byte enables (LBE[3:0]#), 26 address lines (LA[27:2]), and 32-, 16-, or 8-bit data lines (LAD[31:0]).

Read Ahead Mode. The PCI 9052 supports read ahead mode, where prefetched data can be read from the PCI 9052 internal FIFO instead of the local side. Address must be subsequent to previous address and 32-bit aligned (next address = current address + 4).

Bus drivers. All control, address, and data signals generated by the PCI 9052 directly drive the PCI and local bus, without external drivers.

Serial EEPROM interface. The PCI 9052 contains a serial EEPROM interface, used to load configuration information. This is useful for loading information unique to a particular adapter (such as Network ID, Vendor ID, and chip selects).

Note: Serial *EEPROM is required to switch the PCI 9052 into ISA interface mode.*

Four local chip selects. The PCI 9052 provides up to four local chip selects. Base address and range of each chip select are independently programmable from the serial EEPROM or host.

Five Local Address Spaces. Base address and range of each Local Address Space are independently programmable from the serial EEPROM or host.

Big/Little Endian byte swapping. The PCI 9052 supports Big and Little Endian byte ordering. The PCI 9052 also supports Big Endian byte lane mode to redirect the current word/byte lane during 16- or 8-bit local bus operation.

Read/write strobe delay and write cycle hold. Read and Write (RD# and WR#) signals can be delayed from the beginning of cycle for legacy interfaces (such as ISA bus).

Local bus wait states. In addition to LRDYi# (local ready input) handshake signal for variable wait state generations, the PCI 9052 has an internal wait state(s) generator (R/W address to data, R/W data-to-data, and R/W data-to-address).

Programmable prefetch counter. The local bus prefetch counter can be programmed for 0 (no prefetch), 4, 8, 16, or continuous (prefetch counter turned off) Prefetch mode. The prefetched data can be used as cached data if a consecutive address is used (must be longword (Lword) aligned).

Delayed Read mode. The PCI 9052 supports PCI Specification 2.1 Delayed Read with

- PCI Read with Write Flush Mode
- PCI Read No Flush Mode
- PCI Read No Write Mode
- PCI Write Mode

PCI Read/Write request time out Timer. The PCI 9052 has a programmable PCI Target Retry Delay Timer, which, when expired, generates a RETRY to the PCI bus.

ISA mode Interface Logic on-board. The PCI 9052 supports single cycle reads/writes for 8-, 16-bit memory

and I/O-mapped accesses from the PCI bus to ISA bus. Space 0 and Space 1 are used in conjunction with memory and I/O-mapped accesses. Refer to Section 4, "ISA Interface Mode," on how to use the PCI 9052 in ISA mode.

PCI LOCK mechanism. The PCI 9052 supports PCI target LOCK sequences. A PCI master can obtain exclusive access to the PCI 9052 device by locking to the PCI 9052.

The PCI bus transfers up to 132 MB/sec.

Low power CMOS in 160-pin plastic QFP (PQFP) package.

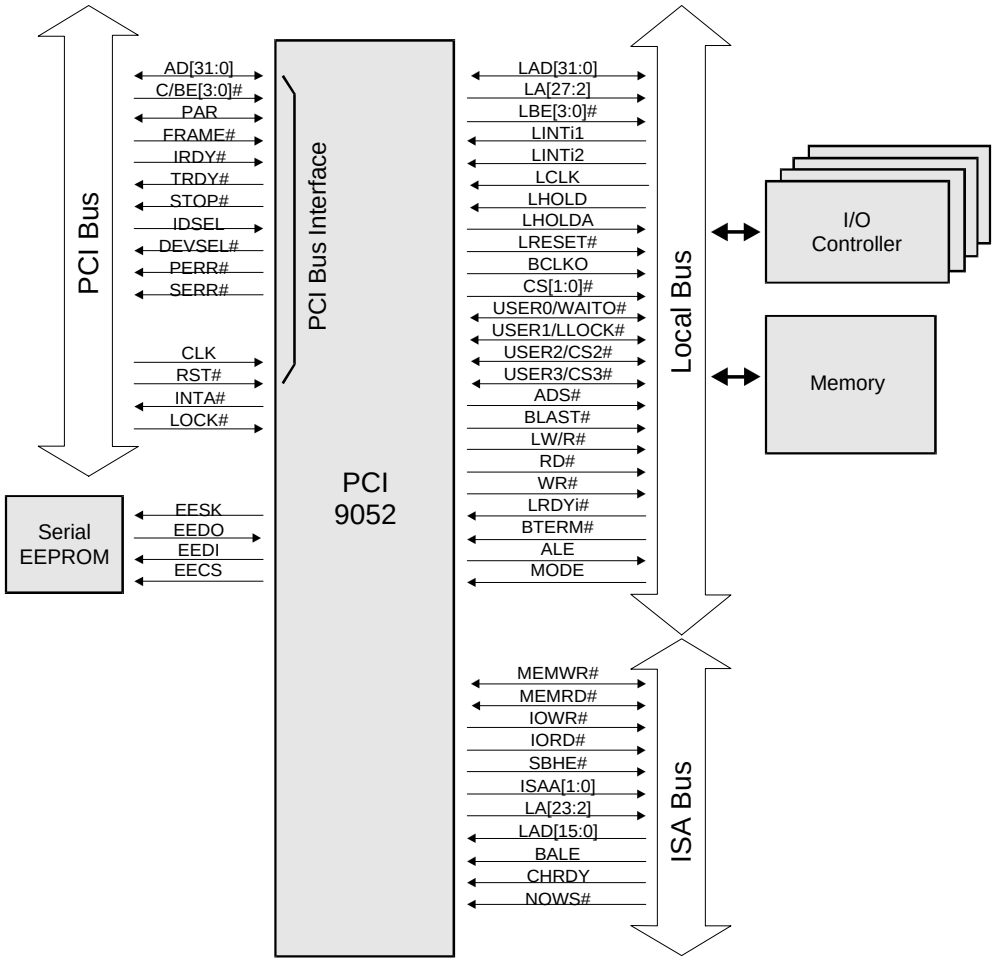


Figure 1-1. PCI 9052 Signal Interfaces

2. BUS OPERATION

2.1 PCI Bus Cycles

The PCI 9052 is PCI Specification 2.1 compliant.

2.1.1 PCI Target Command Codes

As a target, the PCI 9052 allows access to the PCI 9052 internal registers and the local bus, using commands listed in Table 2-1.

Table 2-1. Target Command Codes

Command Type	Code(C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)

All read or write accesses to the PCI 9052 can be byte, word, or Lword accesses. All memory commands are aliased to basic memory commands. All I/O accesses to the PCI 9052 are decoded to a Lword boundary. Byte enables are used to determine which bytes are read from or written to. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

2.2 Local Bus Cycles

2.2.1 Local Bus Slave

Not supported. No Direct Master capability. Internal registers are not readable or writable from the local side. The internal registers are accessible from the Host CPU on the PCI bus or from serial EEPROM.

2.2.2 Local Bus Master

The PCI 9052 is master of the local bus.

2.2.2.1 Ready/Wait-State Control

If LRDYi# input is disabled, external LRDYi# input has no effect on wait states for a local access. Wait-state counter internally generates wait states between address-to-data, data-to-data, and data-to-address cycles. The wait-state counter is initialized with its configuration register value at the start of each data access.

With LRDYi# input enabled, the PCI 9052 will not monitor the LRDYi# signal until the wait-state counter reaches 0. The LRDYi# input then controls the number of additional wait states. (Refer to Figure 2-1 and Figure 2-2.)

The BTERM# input is not sampled until wait-state counter is 0.

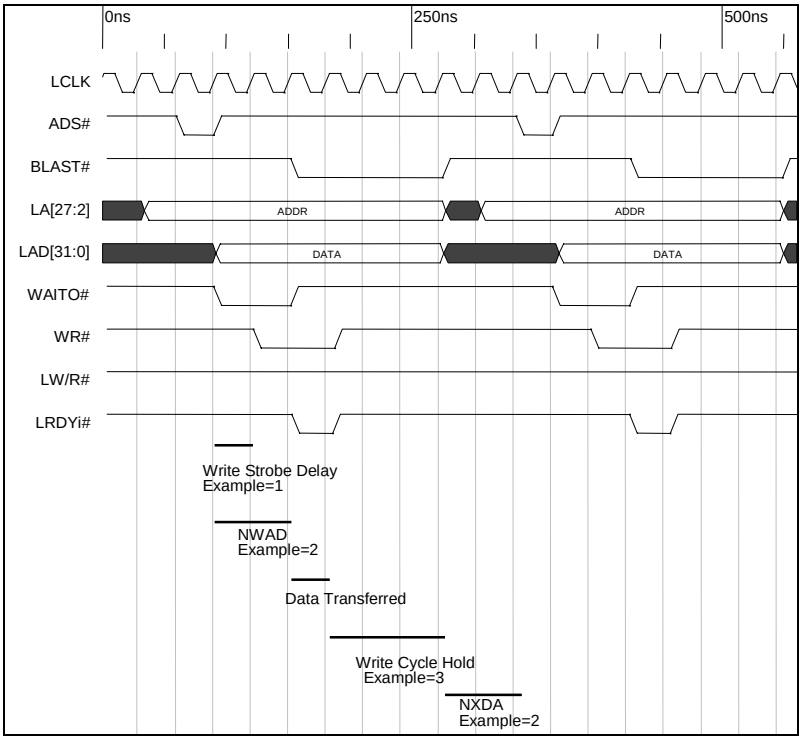


Figure 2-1. PCI 9052 Single Cycle Write

Note: *NWDD is only relevant in a burst cycle, where it determines the wait state between successive data cycles.*

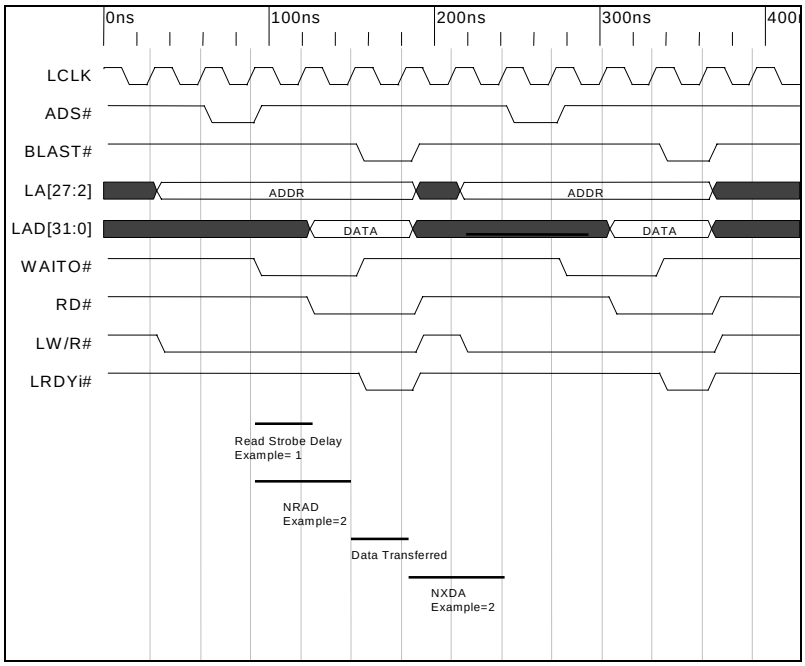


Figure 2-2. PCI 9052 Single Cycle Read

Note: *NRDD is only relevant in a burst cycle, where it determines the wait state between successive data cycles.*

2.2.2.2 Burst Mode and Continuous Burst Mode (Bterm "Burst Terminate" Mode)

2.2.2.2.1 Burst Mode

If bursting is enabled and Bterm input not enabled, the PCI 9052 bursts as follows: Starts on any boundary and continues up to an address boundary, as described in Table 2-2. After transferring the data at the boundary, the PCI 9052 generates a new address cycle (ADS#).

Table 2-2. Burst Mode Boundaries

Bit Bus	Boundary
32	Four Lwords or up to a quad Lword boundary (LA3, LA2 = 11)
16	Four words or up to a quad word boundary (LA2, LA1 = 11)
8	Four bytes or up to a quad byte boundary (LA1, LA0 = 11)

2.2.2.2.2 Continuous Burst Mode (Bterm "Burst Terminate" Mode)

Bterm mode enables the PCI 9052 to perform long bursts to devices that can accept longer than four Lword bursts. The PCI 9052 generates one address cycle, then continues to burst data. If a device requires a new address cycle after a certain address boundary, it can assert BTERM# input to cause the PCI 9052 to generate a new address cycle. BTERM# input is a ready input that acknowledges the current data transfer and requests that a new address cycle be generated (ADS#), which is the address for next data transfer. Enable Bterm mode and the PCI 9052 asserts BLAST# only if the FIFOs become FULL or EMPTY, or a transfer is complete.

Partial Lwords Accesses. Lword accesses (in which not all byte enables are asserted) break into single address and data cycles.

Table 2-3. Partial Lword Accesses

Bus Region Descriptor Register Bits		
Burst Enable	Bterm Enable	Result (Number of Transfers)
0	0	Single Cycle (Default)
0	1	Single Cycle
1	0	Burst Mode—Four Lwords at a time
1	1	Continuous Burst Mode—Burst until Bterm input is asserted (refer to above descriptions)

2.2.2.3 Recovery States

In Non-Multiplexed mode, the PCI 9052 uses NXDA (data-to-address wait states) value in the bus region descriptor register to determine how many recovery states to insert between last data transfer and next address cycle. This value can be programmed between zero and three clock cycles.

In Multiplexed mode, the PCI 9052 inserts a minimum of one recovery state between last data transfer and next address cycle. Add recovery states by programming values greater than one into NXDA bits of the bus region descriptor register.

2.2.2.4 Direct Slave Write Access to 8- and 16-Bit Bus

For direct slave writes/reads, only bytes specified by a PCI bus master are written/read. Access to an 8- or 16-bit bus results in the PCI bus Lword being broken into multiple local bus transfers. For each transfer, byte enables are encoded to provide local address bits LA[1:0].

Do not use direct PCI access to an 8-bit bus with nonadjacent byte enables in a PCI Lword. Nonadjacent byte enables cause an incorrect LA[1:0] address sequence when bursting to memory. Therefore, for each Lword written to an 8-bit bus, the PCI 9052 does not write data after the first gap. Direct PCI accesses to an 8-bit bus with nonadjacent byte enables are not terminated with a Target Abort.

Therefore, for nonadjacent bytes (illegal byte enables), the PCI master must perform single cycles.

2.2.2.5 Local Bus Little/Big Endian

The PCI bus is a Little Endian bus, where data is Lword aligned to lowermost byte lane. Byte 0 (address 0) appears in AD[7:0], Byte 1 appears in AD[15:8], Byte 2 appears in AD[23:16], and Byte 3 appears in AD[31:24].

The PCI 9052 local bus can be programmed to operate in Big or Little Endian mode. In Big Endian mode, the PCI 9052 transposes data byte lanes.

Transfer data as follows:

32-Bit Local Bus. Data is Lword aligned to the uppermost byte lane. Byte lanes and burst orders are listed in Table 2-4 and illustrated in Figure 2-3.

Table 2-4. Upper Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

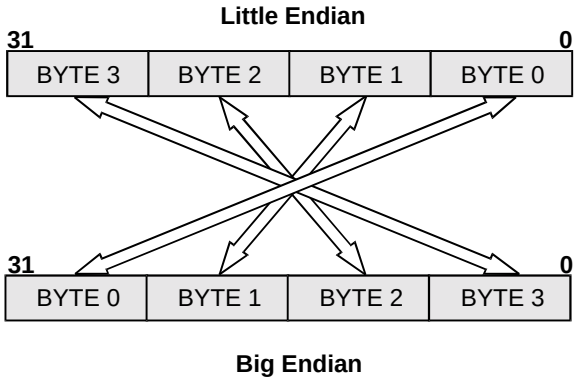


Figure 2-3. Big/Little Endian—32-Bit Local Bus

16-Bit Local Bus. For a 16-bit local bus, the PCI 9052 can be programmed to use the upper or lower word lane. Byte lanes and burst order are listed in Table 2-5 and Table 2-6 and illustrated in Figure 2-4.

Table 2-5. Upper Word Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24], Byte 1 appears on Local Data [23:16]
Second transfer	Byte 2 appears on Local Data [31:24], Byte 3 appears on Local Data [23:16]

Table 2-6. Lower Word Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [15:8], Byte 1 appears on Local Data [7:0]
Second transfer	Byte 2 appears on Local Data [15:8], Byte 3 appears on Local Data [7:0]

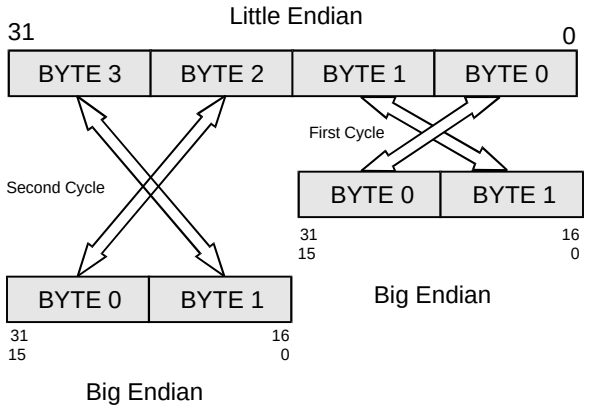


Figure 2-4. Big/Little Endian—16-Bit Local Bus

8-Bit Local Bus. For an 8-bit local bus, the PCI 9052 can be programmed to use the upper or lower byte lane. Byte lanes and burst order are listed in Table 2-7 and Table 2-8 and illustrated in Figure 2-5.

Table 2-7. Upper Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
Second transfer	Byte 1 appears on Local Data [31:24]
Third transfer	Byte 2 appears on Local Data [31:24]
Fourth transfer	Byte 3 appears on Local Data [31:24]

Table 2-8. Lower Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [7:0]
Second transfer	Byte 1 appears on Local Data [7:0]
Third transfer	Byte 2 appears on Local Data [7:0]
Fourth transfer	Byte 3 appears on Local Data [7:0]

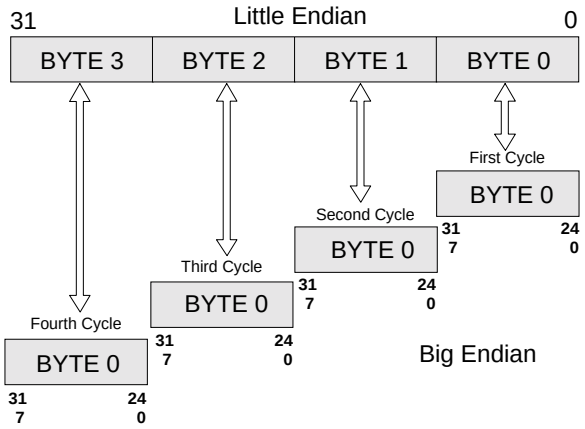


Figure 2-5. Big/Little Endian—8-Bit Local Bus

For each of the following transfer types, the PCI 9052 local bus can be independently programmed to operate in Little Endian or Big Endian mode:

- Direct Slave PCI access to Local Address Space 0
- Direct Slave PCI access to Local Address Space 1
- Direct Slave PCI access to Local Address Space 2
- Direct Slave PCI access to Local Address Space 3
- Direct Slave PCI access to Expansion ROM Space

2.2.2.6 Chip Select x Base Registers

The PCI 9052 includes the ability to provide Chip Select control signals to four devices on the local bus side of the PCI 9052. This eliminates the need to add address decoding circuitry on the adapter card. Without this feature, the user must add address decoding logic for each Chip Select required. This circuitry would then have to monitor the address bus and generate a chip select signal(s).

There are four Chip Select x Base registers. These registers control the four chip select pins on the PCI 9052, respectively. For example, Chip Select 0 Base Address Register controls CS0# (pin 130), Chip Select 1 Base Address Register controls CS1# (pin 131), and so forth.

The Chip Select x Base registers serve three purposes:

1. To enable or disable chip select functions within the PCI 9052. If enabled, the Chip Select signal is active if the address on the address line falls within the address specified by the range and base address. If disabled, the Chip Select signal is not active.
2. To set range or length of addresses at which the Chip Select signal(s) are active.
3. To set base address at which the range starts.

To program the Chip Select x Base registers, there are three rules that must be followed:

1. Range must be a power of 2.
2. Base address must be a multiple of the range
3. Multiple Chip Select x Base registers, if used, are programmed to not overlap one another.

The 28-bit Chip Select x Base register is programmed as listed in Table 2-9.

Table 2-9. Chip Select x Base Register Signal Programming

MSB=27						LSB=0
XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXY

Where the Y bit (bit 0) enables or disables the chip select signal. X bits are used to determine the length and base address of where the CS# pin is asserted. To program the base and length, the X bits are set as follows:

Length or range of the device is equal to the first bit set above the Y bit. Determined by setting bit in the register equal to the exponent in the exponential representation of the range. The bit is counted up, starting at the Y bit, where the Y bit is counted as 1.

Base address is determined by the bit or bits set above the range bit. Multiple of the range. Number uses all of the bits in register above the bit set to determine the range.

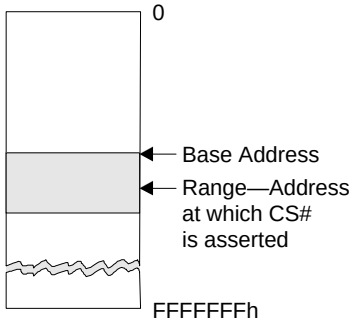


Figure 2-6. Chip Select Base Address and Range

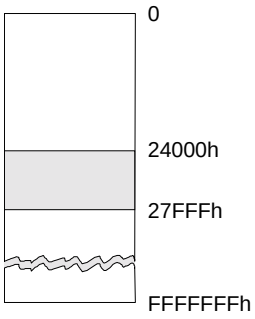
2.2.2.6.1 Procedure

The following procedure describes how to use the Chip Select x Base registers.

1. Determine the range in hex. Convert this number to a power of two. Range must be a power of two (for example, 2^1, 2^2, 2^3, 2^{16}, and so forth.)
2. Set the bit in the Chip Select x Base register to determine the range. Use exponent of the range to set the bit in the Chip Select x Base register. In a binary representation of the Chip Select x Base register, count left, starting at the Y bit, where Y is one. Only one bit may be set.
3. Determine base address. It is recommended to use hex numbers for the base address. Base address must be a multiple of the range.
4. Determine base address multiplier. Divide range into the base address in hex:

   (base address)/(range)=(base address multiplier)
5. Convert base address multiplier to binary.
6. Set base address multiplier bits directly above the range bit in the Chip Select x Base register.

Example: Suppose a 16K SRAM device must be attached to the local bus and a chip select must be provided. The base address will be 24000h. The memory map is as follows:



1. Determine the range in hex and convert the number to a power of 2 (for example, 16K is equivalent to 4000h, or 2^{14} bits).
2. Set the bit in the Chip Select x Base register to determine the range. Set the 14^{th} bit to 1.

MSB=27						LSB=0
0000	0000	0000	0010	0000	0000	0000

1. Determine the base address (for example, 24000h).
2. Determine the base address multiplier. Divide the range into the base address in hex (for example, 24000h/4000h=9h).
3. Convert the base address multiplier to binary (for example, 1001b).
4. Set the base address multiplier bits directly above the range bit in the Chip Select x Base register.

		Base Address				
			Range			
MSB=27						LSB=0
0000	0000	0010	0110	0000	0000	0000

A complete example of setting the Chip Select x Base register with a range of 4000h and a base address of 24000h, and enabled is as follows:

MSB=27						LSB=0
0000	0000	0010	0110	0000	0000	0001

3. FUNCTIONAL DESCRIPTION

3.1 PCI 9052 Initialization

During power up, PCI RST# signal resets default values of the PCI 9052 internal registers. In return, the PCI 9052 outputs the local reset signal (LRESET#) and checks for existence of the serial EEPROM. If a serial EEPROM is installed, and the first 16-bit word is not FFFF, the PCI 9052 loads the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9052 configuration registers can be written only by the optional serial EEPROM or PCI host processor. During the serial EEPROM initialization, the PCI 9052 response to PCI target accesses is RETRYs.

3.2 RESET

3.2.1 PCI Bus Input RST#

The PCI bus RST# input causes all PCI bus outputs to float, resets the entire PCI 9052, and asserts local reset output LRESET#.

3.2.2 Software Reset

A host on the PCI bus can set the software reset bit in Miscellaneous Control Register (CNTRL; 50h) to reset the PCI 9052 and assert LRESET# output. Contents of the PCI and local configuration registers are not reset. When the software reset bit is set, the PCI 9052 responds only to configuration registers accesses, and not to local bus accesses. The PCI 9052 remains in this reset condition until the PCI host clears the software reset bit.

3.2.3 Local Bus Output LRESET#

LRESET# is asserted when the PCI bus RST# input is asserted (4 to 10 ns delay) or bit 30 (software reset bit) in Miscellaneous Control Register (CNTRL; 50h) is set to 1.

3.3 Serial EEPROM

After reset, the PCI 9052 attempts to read serial EEPROM to determine its presence. An active low start bit indicates serial EEPROM is present. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.) If the first word in serial EEPROM is not FFFF, then the PCI 9052 assumes the device is not blank, and continues reading.

Serial EEPROM first stores the most significant bit of each 32-bit word. (The first bit in serial EEPROM is bit 15 of the Device ID.) 25 32-bit words are sequentially stored in the serial EEPROM (such as National NM93CS46 or compatible).

Note: *2K-bit devices, such as 93CS56, are not compatible.*

A host on the PCI bus can read or program serial EEPROM. Bits [29:24] of Miscellaneous Control Register (CNTRL: 50h) control the PCI 9052 pins, enabling reading or writing of serial EEPROM bits. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.)

To reload serial EEPROM data into the PCI 9052 Internal registers, write 1 to bit 29 of register (CNTRL; 50h).

To read/write to the serial EEPROM:

1. Enable serial EEPROM CS[3:0]# by writing 1 to bit 25 of the register (CNTRL; 50h).
2. Generate serial EEPROM clock by writing 0 and then 1. Data is read or written during the zero-to-one transition (refer to bit 24).
3. Send the command code to serial EEPROM.
4. If serial EEPROM is present, a 0 value is returned as a start bit after the command code.
5. Read or write data.
6. Write 0 to bit 25 to end serial EEPROM access (serial EEPROM CS[3:0]# pin will go low).

The serial EEPROM load sequence, listed in Table 3-1, uses the following abbreviations:

MSW = Most Significant Word Bits [31:16]
LSW = Least Significant Word Bits [15:0]

Note: *The PCI 9052 does not support serial EEPROMs that do not support sequential read and write (such as 93C46).*

3.3.1 Serial EEPROM Load Sequence

Table 3-1. Serial EEPROM Load Sequence

Note: *Serial EEPROM value shown is the register value used on a demo board.*

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Register Description
0h	PCI 02h	9050	Device ID.
2h	PCI 00h	10B5	Vendor ID.
4h	PCI 0Ah	0680	Class Code.
6h	PCI 08h	000x	Class code (revision is not loadable).
8h	PCI 2Eh	9050	Subsystem ID.
Ah	PCI 2Ch	10B5	Subsystem Vendor ID.
Ch	PCI 3Eh	xxxx	(Maximum Latency and Minimum Grant are not loadable.)
Eh	PCI 3Ch	01xx	Interrupt Pin (Interrupt Line Routing is not loadable).
10h	LOCAL 02h	0FFE	MSW of Range for PCI to Local Address Space 0.
12h	LOCAL 00h	0000	LSW of Range for PCI to Local Address Space 0.
14h	LOCAL 06h	0FFE	MSW of Range for PCI to Local Address Space 1.
16h	LOCAL 04h	0000	LSW of Range for PCI to Local Address Space 1.
18h	LOCAL 0Ah	0FFF	MSW of Range for PCI to Local Address Space 2.
1Ah	LOCAL 08h	0000	LSW of Range for PCI to Local Address Space 2.
1Ch	LOCAL 0Eh	0FFC	MSW of Range for PCI to Local Address Space 3.
1Eh	LOCAL 0Ch	0000	LSW of Range for PCI to Local Address Space 3.
20h	LOCAL 12h	0000	MSW of Range for PCI to Local Expansion ROM.
22h	LOCAL 10h	0000	LSW of Range for PCI to Local Expansion ROM.
24h	LOCAL 16h	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 0.
26h	LOCAL 14h	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 0.
28h	LOCAL 1Ah	0002	MSW of Local Base Address (Remap) for PCI to Local Address Space 1.
2Ah	LOCAL 18h	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 1.
2Ch	LOCAL 1Eh	0004	MSW of Local Base Address (Remap) for PCI to Local Address Space 2.
2Eh	LOCAL 1Ch	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 2.
30h	LOCAL 22h	0008	MSW of Local Base Address (Remap) for PCI to Local Address Space 3.
32h	LOCAL 20h	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 3.
34h	LOCAL 26h	0010	MSW of Local Base Address (Remap) for PCI to Local Expansion ROM.
36h	LOCAL 24h	0000	LSW of Local Base Address (Remap) for PCI to Local Expansion ROM.

Table 3-1. Serial EEPROM Load Sequence (continued)

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Register Description
38h	LOCAL 2Ah	0080	MSW of Bus Region Descriptors for Local Address Space 0.
3Ah	LOCAL 28h	0026	LSW of Bus Region Descriptors for Local Address Space 0.
3Ch	LOCAL 2Eh	0080	MSW of Bus Region Descriptors for Local Address Space 1.
3Eh	LOCAL 2Ch	003F	LSW of Bus Region Descriptors for Local Address Space 1.
40h	LOCAL 32h	0040	MSW of Bus Region Descriptors for Local Address Space 2.
42h	LOCAL 30h	0037	LSW of Bus Region Descriptors for Local Address Space 2.
44h	LOCAL 36h	5421	MSW of Bus Region Descriptors for Local Address Space 3.
46h	LOCAL 34h	38E9	LSW of Bus Region Descriptors for Local Address Space 3.
48h	LOCAL 3Ah	0000	MSW of Bus Region Descriptors for Expansion ROM Space.
4Ah	LOCAL 38h	0000	LSW of Bus Region Descriptors for Expansion ROM Space.
4Ch	LOCAL 3Eh	0004	MSW of Chip Select (CS) 0 Base and Range Register.
4Eh	LOCAL 3Ch	0001	LSW of Chip Select (CS) 0 Base and Range Register.
50h	LOCAL 42h	000A	MSW of Chip Select (CS) 1 Base and Range Register.
52h	LOCAL 40h	0001	LSW of Chip Select (CS) 1 Base and Range Register.
54h	LOCAL 46h	0000	MSW of Chip Select (CS) 2 Base and Range Register.
56h	LOCAL 44h	0000	LSW of Chip Select (CS) 2 Base and Range Register.
58h	LOCAL 4Ah	0004	MSW of Chip Select (CS) 3 Base and Range Register.
5Ah	LOCAL 48h	8001	LSW of Chip Select (CS) 3 Base and Range Register.
5Ch	LOCAL 4Eh	0000	MSW of Interrupt Control/Status Register.
5Eh	LOCAL 4Ch	0000	LSW of Interrupt Control/Status Register.
60h	LOCAL 52h	0005	MSW of serial EEPROM Control and Miscellaneous Control Register.
62h	LOCAL 50h	4291	LSW of serial EEPROM Control and Miscellaneous Control Register.

3.4 Internal Register Access

The PCI 9052 chip provides several internal registers, allowing maximum flexibility in bus interface design and performance. Register types are as follows:

- **PCI registers** (accessible from the PCI bus and serial EEPROM)
- **Local configuration registers** (accessible from the PCI bus and serial EEPROM)

Note: *Local Configuration Base Address Register access can be limited to memory-mapped or I/O-mapped. Access can also be disabled by way of bits [13:12] of the register at (CNTRL; 50h).*

3.4.1 Internal Registers

Device and Vendor ID. There are two sets of device and vendor IDs. Device and Vendor ID are located at offset 0 of the PCI Configuration Registers. Subsystem Vendor ID and Subsystem Device ID are at offset 2Ch of the PCI configuration Registers. Device ID and Vendor ID identify the particular device, and manufacturer of device. Subsystem Vendor ID and Subsystem ID provide a way to distinguish between vendors of the PCI interface chip and manufacturer of add-in board using the PCI chip.

Status Register. Contains information of the PCI bus-related events.

Command Register. Controls the ability of a device to respond to PCI accesses. It controls whether the device responds to I/O space or memory space accesses.

Class Code Register. Identifies the general function of the device. Refer to the PCI Specification for further details.

Revision ID Register. Value read from this register represents current silicon revision of the PCI 9052.

Header Type. Defines the format of device configuration header and whether the device is single-function or multifunction.

Cache Line Size. Defines system cache line size in units of 32-bit words.

PCI Base Address Register for Memory Accesses to Local Configuration Registers. System BIOS uses this register to assign a segment of the PCI address space for memory accesses to the PCI 9052 Local Configuration Registers. PCI address range occupied by these configuration registers fixes at 128 bytes. During initialization, host writes FFFFFFFF to this register, then reads back FFFFFF70, determining the required memory space of 128 bytes. Host then writes the base address to bits [31:7].

PCI Base Address Register for I/O Accesses to Local Configuration Registers. System BIOS uses this register to assign a segment of the PCI address space for I/O accesses to the PCI 9052 Local Configuration Registers. PCI address range occupied by these configuration registers fixes at 128 bytes. During initialization, host writes FFFFFFFF to this register, then reads back FFFFFF71, determining a required 128 bytes of I/O space. Host then writes the base address to bits [31:7].

PCI Base Address Register for Accesses to Local Address Space 0 (also true for Space 1, 2, and 3). System BIOS uses this register to assign a segment of the PCI address space for accesses to Local Address Space 0. PCI address range occupied by this space is determined by Local Address Space 0 Range Register. During initialization, host writes FFFFFFFF to this register, then reads back a value determined by the range. Host then writes the base address to the upper bits of this register.

PCI Expansion ROM Base Address Register. System BIOS uses this register to assign a segment of the PCI address space for accesses to the Expansion ROM. PCI address range occupied by this space is determined by Expansion ROM Range Register. During initialization, host writes FFFFFFFF to this register, then reads back a value determined by the range. Host then writes the base address to upper bits of this register. Address decoding for expansion ROM can be enabled through the serial EEPROM by writing 1 to (EROMRR; 10h), bit 0.

PCI Interrupt Line Register. Identifies where the interrupt line of the device connects on interrupt controller(s) of system.

PCI Interrupt Pin Register. Specifies the interrupt request pin (if any) to be used.

3.4.2 PCI Bus Access to Internal Registers

The PCI 9052 configuration registers are accessed from the PCI bus by way of a configuration type 0 cycle.

The PCI 9052 local configuration registers are accessed by one of the following:

- A memory cycle, with the PCI bus address matching the base address specified in PCI Base Address Register for Memory Accesses to Local Configuration Registers (PCIBAR0; 10h)
- An I/O cycle, with the PCI bus address matching the base address specified in PCI Base Address Register for I/O Accesses to Local Configuration Registers (PCIBAR1; 14h)

All PCI read or write accesses to the PCI 9052 registers can be byte, word, or Lword accesses. Memory accesses to the PCI 9052 registers can be burst or non-burst. The PCI 9052 responds with a PCI Disconnect for all I/O accesses to the PCI 9052 registers.

3.5 Direct Data Transfer Modes

PCI host processor can directly access devices on the local bus for reads and writes. Configuration registers within the PCI 9052 control decoding and remapping of these accesses to Local Address Space. The read and write FIFOs enable high-performance bursting on the local and PCI buses.

3.5.1 Direct Slave Operation (PCI Master to Local Bus Access)

The PCI 9052 supports memory-*mapped* burst transfer accesses and I/O-*mapped* single transfer accesses to the local bus from the PCI bus. PCI Base Address registers are provided to determine adapter location in PCI memory and I/O space. In addition, local mapping registers are provided to allow address translation from the PCI address space to Local Address Space.

The PCI 9052 disconnects after one transfer for all Direct Slave I/O accesses. For single cycle Direct Slave reads, the PCI 9052 reads a single local bus Lword. For Direct Slave memory accesses, burst read pre-fetching is enabled or disabled through Local Address Space Bus Region Descriptor Registers. If read prefetching is disabled, the PCI 9052 disconnects after one read transfer. If prefetching is enabled, read prefetch size can be programmed through Local Address Space Bus Region Descriptor Registers.

The PCI 9052 can be programmed though the Miscellaneous Control Register (CNTRL; 50h) to perform delayed reads, as specified in PCI Specification v2.1.

3.5.1.1 PCI 2.1 Mode

The PCI 9052 can be programmed through the Local Arbitration and PCI Mode Register to perform delayed reads, as specified in PCI specification v2.1.

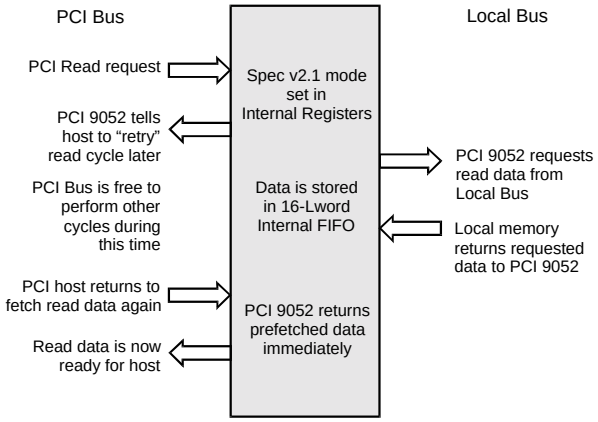


Figure 3-1. PCI Specification v2.1 Delayed Reads

Note: *The figure represents a sequence of bus cycles.*

In addition to delayed read, the PCI 9052 supports the following in PCI specification v2.1 features.

- No write while read is pending (RETRY for reads)
- Write and flush pending read

The PCI 9052 also supports Read Ahead mode (refer to Figure 3-2), where prefetched data can be read from the PCI 9052 internal FIFO instead of from the local side. The address must be subsequent to the previous address and must be 32-bit aligned (next address = current address + 4).

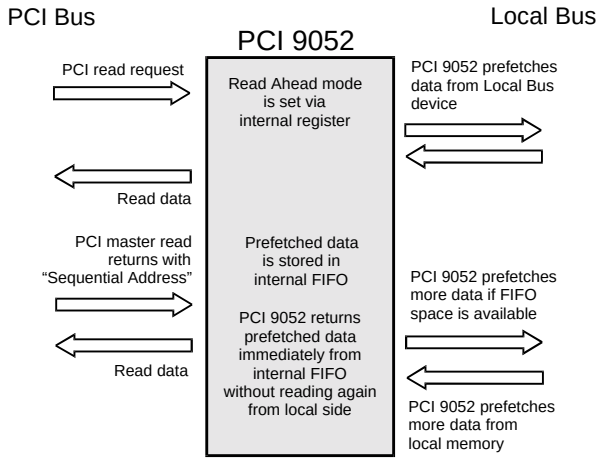


Figure 3-2. PCI 9052 Read Ahead Mode

Note: *The figure represents a sequence of bus cycles.*

The PCI 9052 can be programmed to keep the PCI bus by generating a wait state(s), de-asserting TRDY#, if the write FIFO becomes full. (Refer to Figure 3-3 and Figure 3-4.)

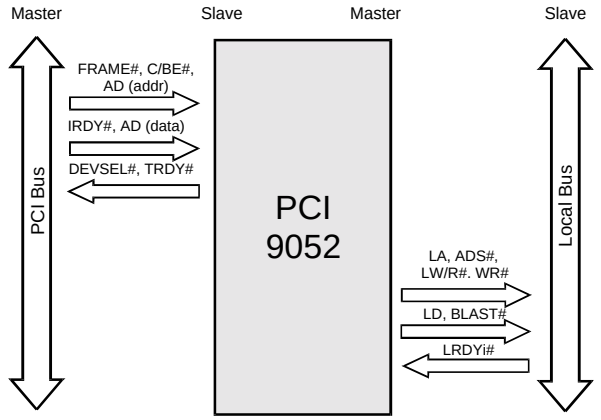


Figure 3-3. Direct Slave Write

Note: *The figure represents a sequence of bus cycles.*

For direct slave writes, the PCI (Master) writes data to the local bus (slave).

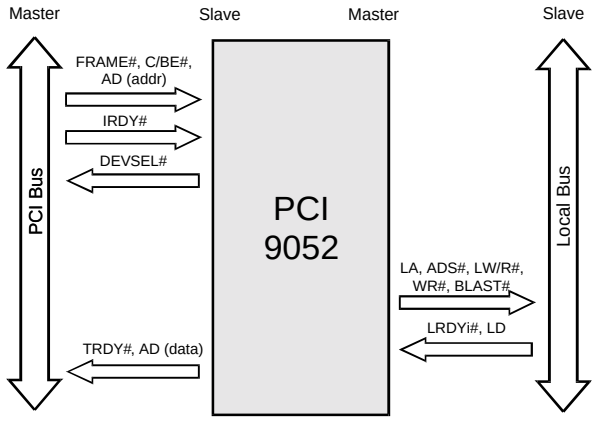


Figure 3-4. Direct Slave Read

Note: *The figure represents a sequence of bus cycles.*

For direct slave reads, the PCI (Master) reads data from the local bus (Slave).

The PCI 9052 supports on-the-fly Endian conversion for Space 0, Space 1, and expansion ROM space. The local bus can be Big/Little Endian by the programmable internal register configuration.

Note: *The PCI bus is always Little Endian.*

3.5.1.2 PCI to Local Address Mapping

Five Local Address Spaces (local spaces 0-3 and expansion ROM) are accessible from the PCI bus. A set of four registers defines each space, defining the local bus characteristics:

- PCI Base Address
- Local Range
- Local Base Address (Remap)
- Local Bus Region Descriptor

Byte Enables (LBE[3:0]#, pins 46-49) are encoded based upon configured bus width:

32-bit bus. Four byte enables indicate which of the four bytes are active during a data cycle:

- LBE3# Byte Enable 3 = LAD[31:24]
- LBE2# Byte Enable 2 = LAD[23:16]
- LBE1# Byte Enable 1 = LAD[15:8]
- LBE0# Byte Enable 0 = LAD[7:0]

16-bit bus. LBE[3,1:0]# are encoded to provide BHE#, LA1, and BLE#:

- LBE3# Byte High Enable (BHE#) = LAD[15:8]
- LBE2# Unused
- LBE1# Address bit 1 = (LA1)
- LBE0# Byte Low Enable (BLE#) = LAD[7:0]

8-bit bus. LBE[1:0]# are encoded to provide LA[1:0]:

- LBE3# Unused
- LBE2# Unused
- LBE1# Address bit 1 = (LA1)
- LBE0# Address bit 0 = (LA0)

Each PCI to Local Address space is defined as part of the reset initialization:

Local bus initialization software. Range specifies which PCI address bits to use to decode a PCI access to local bus space. Each of the bits correspond to an address bit, with bit 31 corresponding to address bit 31. Write 1 to all bits to be included in the decoding. Write 0 to all bits to be ignored.

Remap PCI address into a local address. Bits in this register remap (replace) the PCI address bits used in decoding into the local address bits.

Local Bus Region Descriptor specifies the local bus characteristics, such as bus width, bursting, prefetching, and number of wait states.

PCI Initialization Software. PCI host bus-initialization software determines the required address space by writing a value of all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9052 returns zeros (0) in don't care address bits, specifying the required address space. PCI software then maps Local Address space into the PCI Address space by programming PCI Base Address register.

Example: A 1 MB Local Address Space 02300000h through 023FFFFFh is accessible from the PCI bus at PCI addresses 78900000h through 789FFFFFh.

1. From serial EEPROM sets the Range and Local Base address registers as follows:
   - Range = FFF00000h (1 MB, decode the upper 12 PCI address bits)
   - Local Base Address (remap) = 023XXXXXh (Local Base Address for PCI to local accesses)

2. PCI Initialization software writes all ones (1) to the PCI Base Address, then reads back the value. The PCI 9052 returns a value FFF00000h. PCI software then writes to PCI Base Address register:

    - PCI Base Address = 789XXXXXh (PCI Base Address for access to Local Address space)

For PCI accesses to the local bus, the PCI 9052 has a 16-Lword (64-byte) write FIFO and an 8-Lword (32-byte) read FIFO. The FIFOs enables the local bus to operate independently of the PCI bus. The PCI 9052 can be programmed to return a RETRY response or to throttle TRDY# for PCI bus transactions attempting to write to the PCI 9052 local bus when the write FIFO is full.

For PCI read transactions from the PCI 9052 local bus, the PCI 9052 holds off TRDY# while gathering the local bus Lword to be returned. For read accesses mapped to the PCI memory space, the PCI 9052 prefetches up to four Lwords from the local bus. Unused read data is flushed from the FIFO. For read accesses mapped to the PCI I/O space, the PCI 9052 does not prefetch read data. It breaks each read of the burst cycle into a single address/data cycle on the local bus.

The period of time that the PCI 9052 holds off TRDY# is programmed in the Miscellaneous Control Register (CNTRL; 50h). The PCI 9052 issues a RETRY to the PCI bus master when programmed time period expires. This happens when the PCI 9052 cannot get the data from the local bus and return TRDY# within the programmed time period.

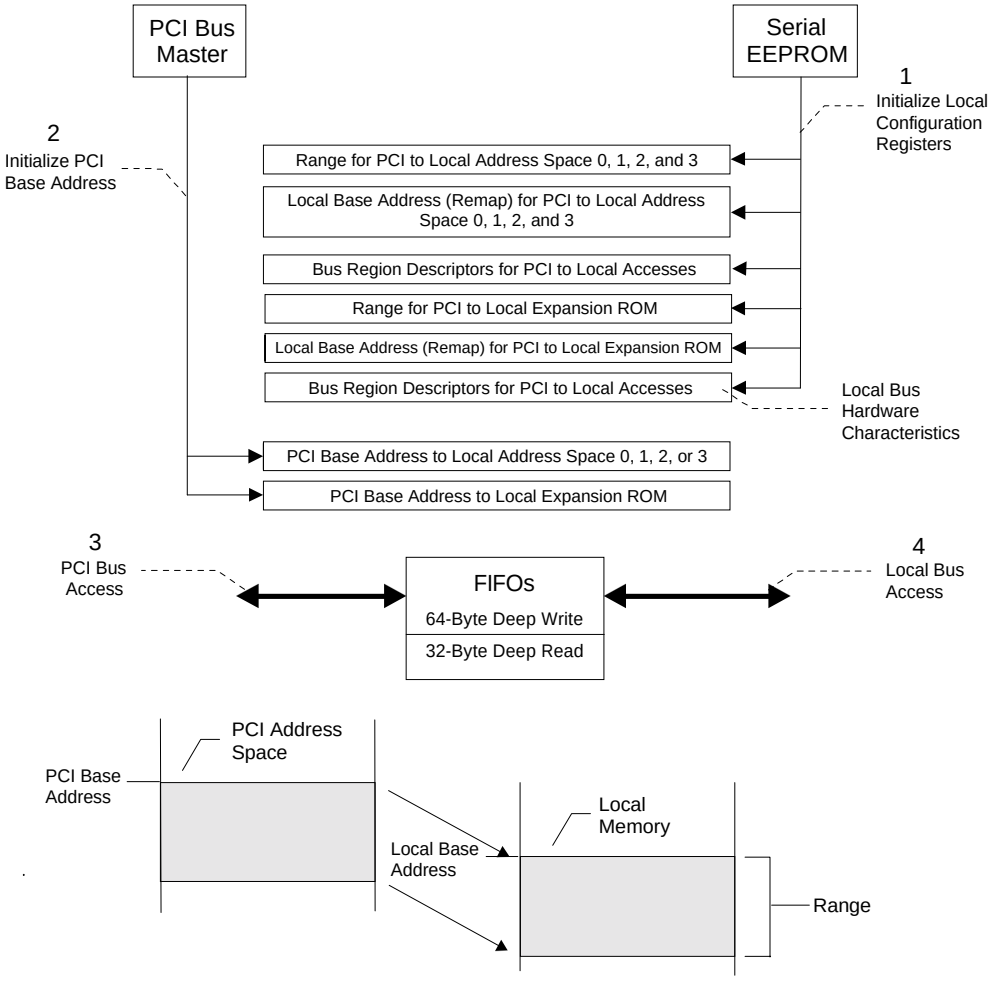


Figure 3-5. PCI Master Direct Access of Local Bus

3.5.1.3 Direct Slave Lock

The PCI 9052 supports direct PCI to local bus exclusive accesses (locked atomic operations). A PCI locked operation to the local bus results in the entire address space 0-3 and expansion ROM space being locked until the PCI bus master releases the spaces. The PCI 9052 asserts LLOCKo# during the first clock of an atomic operation (address cycle) and de-asserts it a minimum of one clock following the last bus access for atomic operation. LLOCKo# is de-asserted after the PCI 9052 detects PCI FRAME#, with PCI LOCK# de-asserted at the same time. (Refer to Section 9, “Timing Diagrams.”) The Miscellaneous Control Register (CNTRL; 50h) enables locked operations.

It is the responsibility of external arbitration logic to monitor LLOCKo# pin and enforce the meaning for an atomic operation. For example, if a local master initiates a locked operation, the local arbiter may choose to not grant use of the local bus to other masters until locked operation is complete.

3.5.1.4 Arbitration

When the PCI bus detects a new transfer request, the PCI 9052 takes control of the local bus. Another device can gain control of the local bus by asserting LHOLD. If the PCI 9052 has no cycles to run, it asserts LHOLDA, transferring control to the external master. If the PCI 9052 needs the local bus before the external master has finished, LHOLDA is de-asserted (preempt condition). The arbiter waits for LHOLD to be de-asserted before taking control of the bus.

3.6 PCI Interrupts (INTA#)

You can generate a PCI interrupt (INTA#) with local interrupt inputs LINTi1 and LINTi2, and the software interrupt (CNTRL register bit 30). Through the PCI 9052 Interrupt Control/Status Register, individual sources of an interrupt can be enabled or disabled. Interrupt Control/Status Register also provides interrupt status for each source of the interrupt.

The PCI 9052 PCI bus interrupt is an asynchronous level output. Clear an interrupt by disabling an interrupt enable bit of a source or by clearing the cause of an interrupt.

3.7 Local Interrupt (LINTi[2:1])

The PCI 9052 provides two local interrupts (LINTi[2:1]). The local interrupts can be used to generate PCI interrupt. LINTi[2:1] supports edge or level trigger, programmable through register (INTCSR; 4Ch).

3.8 PCI SERR# (PCI NMI)

The PCI 9052 generates a SERR# pulse if parity checking is enabled in the PCI Command Register and an address parity error is detected. Through the PCI Command Register, SERR# output is enabled.

4. ISA INTERFACE MODE

4.1 Architecture

A major architectural feature of the PCI 9052 is the inclusion of a glueless ISA logic interface. This provides for a smooth ISA to PCI conversion. It supports 8- and 16-bit wide ISA devices that can be memory or I/O-mapped. Read Ahead mode can be used to improve read data throughput. The PCI 9052 performs only single cycles once ISA interface mode is enabled.

Note: *A serial EEPROM is required to enable the ISA Interface mode.*

4.2 Configuration Methods

Use one of the following methods to configure the PCI 9052 for ISA interface mode.

1. Preprogram serial EEPROM method

   Using the pre-programmer, program the serial EEPROM. Refer to Table 4-1 for appropriate values.

   Note: *LRESET# pin is always an active high signal for ISA mode. Ensure the PCI 9052 mode-pin is set to 0.*

2. On-the-fly method

   From the PCI bus, program the serial EEPROM through the PCI 9052 using the same values as indicated in the preprogramming method.

   Notes: *LRESET# pin changes its polarity from active low to active high in ISA mode. Ensure the PCI 9052 mode pin is set to 0.*

   While in ISA mode, Local Space 2, 3, and Expansion ROM can be configured to operate in Non-multiplexed mode.

Table 4-1. Serial EEPROM Load Sequence

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Register Description
0h	PCI 02h	9050	Device ID.
2h	PCI 00h	10B5	Vendor ID.
4h	PCI 0Ah	0680	Class Code.
6h	PCI 08h	000x	Class code (revision is not loadable).
8h	PCI 2Eh	9050-1	Subsystem ID.
Ah	PCI 2Ch	10B5	Subsystem Vendor ID.
Ch	PCI 3Eh	XXXX	(Maximum Latency and Minimum Grant are not loadable.)
Eh	PCI 3Ch	01xx	Interrupt Pin (Interrupt Line Routing is not loadable).
10h	LOCAL 02h	—	MSW of Range for PCI to Local Address Space 0.
12h	LOCAL 00h	—	LSW of Range for PCI to Local Address Space 0. Bit 0 must be 0 for memory-mapped.
14h	LOCAL 06h	—	MSW of Range for PCI to Local Address Space 1.
16h	LOCAL 04h	—	LSW of Range for PCI to Local Address Space 1. Bit 0 must be 1 for I/O-mapped.
18h	LOCAL 0Ah	—	MSW of Range for PCI to Local Address Space 2.
1Ah	LOCAL 08h	XXXX	LSW of Range for PCI to Local Address Space 2.
1Ch	LOCAL 0Eh	XXXX	MSW of Range for PCI to Local Address Space 3.
1Eh	LOCAL 0Ch	XXXX	LSW of Range for PCI to Local Address Space 3.
20h	LOCAL 12h	XXXX	MSW of Range for PCI to Local Expansion ROM.
22h	LOCAL 10h	XXXX	LSW of Range for PCI to Local Expansion ROM.

Notes: ***The s****erial EEPROM value shown is the register value used on a demo board.*

The serial EEPROM value of "X" represents "don't care."

Table 4-1. Serial EEPROM Load Sequence (continued)

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Register Description
24h	LOCAL 16h	—	MSW of Local Base Address (Remap) for PCI to Local Address Space 0.
26h	LOCAL 14h	—	LSW of Local Base Address (Remap) for PCI to Local Address Space 0.
28h	LOCAL 1Ah	—	MSW of Local Base Address (Remap) for PCI to Local Address Space 1.
2Ah	LOCAL 18h	—	LSW of Local Base Address (Remap) for PCI to Local Address Space 1.
2Ch	LOCAL 1Eh	XXXX	MSW of Local Base Address (Remap) for PCI to Local Address Space 2.
2Eh	LOCAL 1Ch	XXXX	LSW of Local Base Address (Remap) for PCI to Local Address Space 2.
30h	LOCAL 22h	XXXX	MSW of Local Base Address (Remap) for PCI to Local Address Space 3.
32h	LOCAL 20h	XXXX	LSW of Local Base Address (Remap) for PCI to Local Address Space 3.
34h	LOCAL 26h	XXXX	MSW of Local Base Address (Remap) for PCI to Local Expansion ROM.
36h	LOCAL 24h	XXXX	LSW of Local Base Address (Remap) for PCI to Local Expansion ROM.
38h	LOCAL 2Ah	—	MSW of Bus Region Descriptors for Local Address Space 0. Refer to Table 4-2.
3Ah	LOCAL 28h	—	LSW of Bus Region Descriptors for Local Address Space 0. Refer to Table 4-2.
3Ch	LOCAL 2Eh	—	MSW of Bus Region Descriptors for Local Address Space 1. Refer to Table 4-2.
3Eh	LOCAL 2Ch	—	LSW of Bus Region Descriptors for Local Address Space 1. Refer to Table 4-2.
40h	LOCAL 32h	XXXX	MSW of Bus Region Descriptors for Local Address Space 2.
42h	LOCAL 30h	XXXX	LSW of Bus Region Descriptors for Local Address Space 2.
44h	LOCAL 36h	XXXX	MSW of Bus Region Descriptors for Local Address Space 3.
46h	LOCAL 34h	XXXX	LSW of Bus Region Descriptors for Local Address Space 3.
48h	LOCAL 3Ah	XXXX	MSW of Bus Region Descriptors for Expansion ROM Space.
4Ah	LOCAL 38h	XXXX	LSW of Bus Region Descriptors for Expansion ROM Space.
4Ch	LOCAL 3Eh	—	MSW of Chip Select (CS) 0 Base and Range Register. Base address must match Local Space 0 remap address.
4Eh	LOCAL 3Ch	—	LSW of Chip Select (CS) 0 Base and Range Register. Base address must match Local Space 0 remap address.
50h	LOCAL 42h	—	MSW of Chip Select (CS) 1 Base and Range Register. Base address must match Local Space 1 remap address.
52h	LOCAL 40h	—	LSW of Chip Select (CS) 1 Base and Range Register. Base address must match Local Space 1 remap address.
54h	LOCAL 46h	XXXX	MSW of Chip Select (CS) 2 Base and Range Register.
56h	LOCAL 44h	XXXX	LSW of Chip Select (CS) 2 Base and Range Register.
58h	LOCAL 4Ah	XXXX	MSW of Chip Select (CS) 3 Base and Range Register.
5Ah	LOCAL 48h	XXXX	LSW of Chip Select (CS) 3 Base and Range Register.
5Ch	LOCAL 4Eh	—	MSW of Interrupt Control/Status Register. Refer to Table 4-3.
5Eh	LOCAL 4Ch	—	LSW of Interrupt Control/Status Register. Refer to Table 4-3.
60h	LOCAL 52h	—	MSW of Serial EEPROM Control and Miscellaneous Control Register. Refer to Table 4-4.
62h	LOCAL 50h	—	LSW of Serial EEPROM Control and Miscellaneous Control Register. Refer to Table 4-4.

Notes: ***The s****erial EEPROM value shown is the register value used on a demo board.*

The serial EEPROM value of "X" represents "don't care."

4.3 Configuration Notes

Be aware of the following when configuring for ISA interface mode:

- The PCI 9052 pin defaults have not changed for regular Direct Slave accesses. When NC is indicated, this represents a true No Connect.
- To access ISA interface pins, refer to the PCI 9052 Pin Out (C/ISA Mode) diagram (refer to Section 8.3, “PCI 9052 Pin Out”).
- Space 0 is assigned to memory accesses for ISA interface.
- Space 1 is assigned to I/O accesses for ISA interface.
- ISA accesses are active whenever a local address of Space 0 is in the range of CS0#, and a local address of Space 1 is in the range CS1#.
- Standard Slave cycles could be accessed using Space 2, Space 3, and serial EEPROM.

4.4 Configuring Local Registers for ISA Mode

Be aware of the following when configuring local registers for ISA interface mode:

- Serial EEPROM presence must be detected on board for the PCI 9052 to operate in ISA interface mode.
- MODE pin must be set to 0, non-multiplexed bus.
- LAS0RR and LAS1RR registers must be set. Refer to Table 5-26 and Table 5-27.

Note: *Bit 0 should be set to 0 in LAS0RR and to 1 in LAS1RR registers to indicate memory mapping for Space 0, and I/O mapping for Space 1 on the PCI Bus.*

- LAS0BA and LAS1BA registers should be set. Refer to Table 5-31 and Table 5-32.
- LAS0BRD and LAS1BRD registers should be set as listed in Table 4-2.
- CS0BASE and CS1BASE must be set accordingly to the local address of Space 0 and Space 1. Otherwise, the ISA interface is never acknowledged. Refer to Table 5-41 and Table 5-42.
- Set INTCSR registers as listed in Table 4-3.
- Set CNTRL register as listed in Table 4-4.

Table 4-2. LAS0BRD and LAS1BRD Register Settings

Bit	Description	Value after Serial EEPROM Load
0	Burst is disabled on the local bus.	0
1	Ready is enabled. Internal to the PCI 9052.	1
2	BTERM# feature is not used.	X
4:3	Prefetch on the local bus is disabled.	XX
5	Prefetch is disabled.	0
10:6	Refer to the (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor Register and the (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor Register.	—
12:11	No Data-to-Data Wait States.	00
19:13	Refer to registers 28h and 30h.	—
21:20	No Data-to-Data Wait States.	—
23:22	h2 is prohibited from use.	0/1
25:24	Refer to the (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor Register and the (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor Register.	—
27:26	Read strobe is not used.	XX
29:28	Write strobe is not used.	XX
31:30	Write strobe feature is not used.	XX

Table 4-3. INTCSR Register Settings

Bit	Description	Value after Serial EEPROM Load
9:0	Refer to the (INTCSR; 4Ch) Interrupt Control/Status Register.	—
12	ISA_MODE feature enabled. Must be 1.	1

Table 4-4. CNTRL Register Settings

Bit	Description	Value after Serial EEPROM Load
0	Pin 138 is programmed to USER I/O.	0
1	Pin 138 is programmed to be an output.	1
2	USER I/O feature is disabled with ISA_MODE bit.	X
3	Pin 139 is programmed to USER I/O.	0
4	Pin 139 is programmed to be an output.	1
5	USER I/O feature is disabled with the ISA_MODE bit.	X
30:6	Refer to the (CNTRL; 50h) User I/O, PCI Target Response, Serial EEPROM, Initialization Control Register.	—

Note: ***The s****erial EEPROM value of "X" represents "don't care."*

5. REGISTERS

5.1 Register Address Mapping

Table 5-1. PCI Configuration Registers

PCI CFG Register Address	To ensure software compatibility with other versions of PCI 9050 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 24 23 16 15 8 7 0				PCI Writable	Serial EEPROM Writable
00h	Device ID		Vendor ID		N	Y
04h	Status		Command		Y	N
08h	Class Code			Revision ID	N	Y[31:8]
0Ch	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	N
10h	PCI Base Address 0 for Memory-Mapped Configuration Registers				Y	N
14h	PCI Base Address 1 for I/O-Mapped Configuration Registers				Y	N
18h	PCI Base Address 2 for Local Address Space 0				Y	N
1Ch	PCI Base Address 3 for Local Address Space 1				Y	N
20h	PCI Base Address 4 for Local Address Space 2				Y	N
24h	PCI Base Address 5 for Local Address Space 3				Y	N
28h	Cardbus CIS Pointer (Not Supported)				N	N
2Ch	Subsystem ID		Subsystem Vendor ID		N	Y
30h	PCI Base Address for Local Expansion ROM				Y	N
34h	***Reserved***				N	N
38h	***Reserved***				N	N
3Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	Y[15:8]

Table 5-2. Local Configuration Registers

PCI (Offset from Local Base Address)	To ensure software compatibility with other versions of PCI 9050 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 0	PCI and Serial EEPROM Writable
00h	Local Address Space 0 Range	Y
04h	Local Address Space 1Range	Y
08h	Local Address Space 2 Range	Y
0Ch	Local Address Space 3 Range	Y
10h	Local Expansion ROM Range	Y
14h	Local Address Space 0 Local Base Address (Remap)	Y
18h	Local Address Space 1 Local Base Address (Remap)	Y
1Ch	Local Address Space 2 Local Base Address (Remap)	Y
20h	Local Address Space 3 Local Base Address (Remap)	Y
24h	Expansion ROM Local Base Address (Remap)	Y
28h	Local Address Space 0 Bus Region Descriptors	Y
2Ch	Local Address Space 1 Bus Region Descriptors	Y
30h	Local Address Space 2 Bus Region Descriptors	Y
34h	Local Address Space 3 Bus Region Descriptors	Y
38h	Expansion ROM Bus Region Descriptors	Y
3Ch	Chip Select 0 Base Address	Y
40h	Chip Select 1 Base Address	Y
44h	Chip Select 2 Base Address	Y
48h	Chip Select 3 Base Address	Y
4Ch	Interrupt Control/Status	Y
50h	Serial EEPROM Control, PCI Slave Response, User I/O Control, Init Control	Y

5.2 PCI Configuration Registers

All registers may be written to or read from byte, word, or Lword accesses.

Table 5-3. (PCIIDR; 00h) PCI Configuration ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies manufacturer of the device. Defaults to PCI SIG issued Vendor ID of PLX if no serial EEPROM is present.	Yes	Serial EEPROM	10B5h
31:16	Device ID. Identifies particular device. Defaults to PLX part number for the PCI interface chip if no serial EEPROM is present.	Yes	Serial EEPROM	9050

Table 5-4. (PCICR; 04h) PCI Command Register

Bit	Description	Read	Write	Value after Reset
0	I/O Space. Value of 1 allows device to respond to I/O space accesses. Value of 0 disables device from responding to I/O space accesses.	Yes	Yes	0
1	Memory Space. Value of 1 allows device to respond to memory space accesses. Value of 0 disables device from responding to memory space accesses.	Yes	Yes	0
2	Master Enable. Value of 1 allows device to function as a bus master. Value of 0 disables device from generating bus master accesses.	Yes	No	0
3	Special Cycle. **Not Supported.**	Yes	No	0
4	Memory Write/Invalidate. **Not Supported.**	Yes	No	0
5	VGA Palette Snoop. **Not Supported.**	Yes	No	0
6	Parity Error Response. Value of 0 indicates a parity error is ignored and operation continues. Value of 1 indicates parity checking is enabled.	Yes	Yes	0
7	Wait Cycle Control. Controls whether the device does address/data stepping. Value of 0 indicates device never does stepping. Value of 1 indicates device always does stepping. ***Note:*** *Hardcoded to 0.*	Yes	No	0
8	SERR# Enable. Value of 1 enables SERR# driver. Value of 0 disables SERR# driver.	Yes	Yes	0
9	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. Value of 1 indicates fast back-to-back transfers can occur to any agent on the bus. Value of 0 indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.	Yes	No	0
15:10	***Reserved***.	Yes	No	0

Table 5-5. (PCISR; 06h) PCI Status Register

Bit	Description	Read	Write	Value after Reset
6:0	***Reserved***.	Yes	No	0
7	Fast Back-to-Back Capable. Value of 1 indicates adapter can accept fast back-to-back transactions. Value of 0 indicates adapter cannot accept fast back-to-back transactions.	Yes	No	1h
8	Master Data Parity Error Detected. **Not Supported.**	Yes	No	0
10:9	DEVSEL Timing. Indicates timing for DEVSEL# assertion. Value of 01 is medium.	Yes	No	01
11	Target Abort. Value of 1 indicates the PCI 9052 has signaled a target abort. Writing a value of 1 clears bit (0).	Yes	Yes	0
12	Received Target Abort. Value of 1 indicates the PCI 9052 has received a target abort signal. **Not Supported.**	Yes	No	0
13	Received Master Abort. Value of 1 indicates the PCI 9052 has received a master abort signal. Not supported	Yes	No	0
14	Signaled System Error. Value of 1 indicates the PCI 9052 has reported a system error on SERR# signal. Writing a value of 1 clears the error status bit (0).	Yes	Yes	0
15	Detected Parity Error. Value of 1 indicates the PCI 9052 has detected a PCI bus parity error, even if parity error handling is disabled (Parity Error Response bit in the Command Register is clear). To cause a bit to be set, one of these two conditions must exist: 1) The PCI 9052 detected a parity error during a PCI address phase; or, 2) The PCI 9052 detected a data parity error when it was the target of a write. Writing a value of 1 clears bit (0).	Yes	Yes	0

Table 5-6. (PCIREV; 08h) PCI Revision ID Register

Bit	Description	Read	Write	Value after Reset
7:0	Revision ID. The silicon revision of the PCI 9052. ***Note:*** *Hardcoded to 9050.*	Yes	No	Current Revision

Table 5-7. (PCICCR; 09-0Bh) PCI Class Code Register

Bit	Description	Read	Write	Value after Reset
7:0	Specific Register Level Programming Interface (00h). No interface defined.	Yes	Serial EEPROM	00
15:8	Subclass Encoding (80h). Other bridge device.	Yes	Serial EEPROM	80h
23:16	Base Class Encoding. Other bridge Device.	Yes	Serial EEPROM	06h

Table 5-8. (PCICLSR; 0Ch) PCI Cache Line Size Register

Bit	Description	Read	Write	Value after Reset
7:0	System Cache Line Size (in units of 32-bit words). Can be written and read; however, the value has no effect on operation of chip.	Yes	Yes	0

Table 5-9. (PCILTR; 0Dh) PCI Latency Timer Register

Bit	Description	Read	Write	Value after Reset
7:0	PCI Latency Timer. **Not Supported.**	Yes	No	0

Table 5-10. (PCIHTR; 0Eh) PCI Header Type Register

Bit	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies layout of bits 10h through 3Fh in configuration space. Only one encoding 0 is defined. All other encodings are reserved.	Yes	No	0
7	Header Type. Value of 1 indicates multiple functions. Value of 0 indicates a single function.	Yes	No	0

Table 5-11. (PCIBISTR; 0Fh) PCI Built-In Self Test (BIST) Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Built-In Self Test. Value of 0 indicates device has passed its test. **Not Supported.**	Yes	No	0

Table 5-12. (PCIBAR0; 10h) PCI Base Address Register for Memory Accesses to Local Configuration Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space. ***Note:*** *Hardcoded to 0.*	Yes	No	0
2:1	Location of register: 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** ***Note:*** *Hardcoded to 0.*	Yes	No	0
3	Prefetchable. Value of 1 indicates no side effect on reads. ***Note:*** *Hardcoded to 0.*	Yes	No	0
6:4	Memory Base Address. Memory base address for access to the local configuration registers (default 128 bytes). ***Note:*** *Hardcoded to 0.*	Yes	No	0
31:7	Memory Base Address. Memory base address for access to the local configuration registers	Yes	Yes	0

Note: *PCIBAR0 can be enabled or disabled using bits [13:12] in the CNTRL register.*

Table 5-13. (PCIBAR1; 14h) PCI Base Address Register for I/O Accesses to Local Configuration Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space. ***Note:*** *Hardcoded to 1*.	Yes	No	1h
1	***Reserved***.	Yes	No	0
6:2	I/O Base Address. Base address for I/O access to the local configuration registers (default 128 bytes*)*. ***Note:*** *Hardcoded to 0.*	Yes	No	0
31:7	I/O Base Address. Base address for I/O access to the local configuration registers.	Yes	Yes	0

Note: *PCIBAR1 can be enabled or disabled using bits [13:12] in the CNTRL register.*

Table 5-14. (PCIBAR2; 18h) PCI Base Address Register for Memory Access to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space. (Specified in LAS0RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS0RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). Value of 1 indicates no side effects on reads. This bit reflects the value of bit 3 in LAS0RR register, only provides status to the system, and has no effect on operation of the PCI 9052. Associated Bus Region Descriptor Register (LAS0BRD) controls prefetching features of this address space. (Specified in LAS0RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to Local Address Space.	Yes	Yes	0

Note: *PCIBAR2 can be enabled or disabled by setting or clearing bit 0 in the LAS0BA register.*

Table 5-15. (PCIBAR3; 1Ch) PCI Base Address Register for Memory Access to Local Address Space 1

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space. (Specified in LAS1RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS1RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). Value of 1 indicates no side effects on reads. This bit reflects the value of bit 3 in LAS1RR register, only provides status to the system, and has no effect on operation of the PCI 9052. Associated Bus Region Descriptor Register (LAS1BRD) controls prefetching features of this address space. (Specified in LAS1RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to the Local Address Space.	Yes	Yes	0

Note: *PCIBAR3 can be enabled or disabled by setting or clearing bit 0 in the LAS1BA register.*

Table 5-16. (PCIBAR4; 20h) PCI Base Address Register for Memory Access to Local Address Space 2

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space. (Specified in LAS2RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS2RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). Value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in LAS2RR register, only provides status to the system, and has no effect on operation of the PCI 9052. Associated Bus Region Descriptor Register (LAS2BRD) controls prefetching features of this address space. (Specified in LAS2RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to Local Address Space.	Yes	Yes	0

Note: *PCIBAR4 can be enabled or disabled by setting or clearing bit 0 in the LAS2BA register.*

Table 5-17. (PCIBAR5; 24h) PCI Base Address Register for Memory Access to Local Address Space 3

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space. (Specified in LAS3RR register.)	Yes	No	0
2:1	Location of Register (if Memory space): 00 = Locate anywhere in 32-bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64-bit memory address space 11 = ***Reserved*** (Specified in LAS3RR register.) If I/O space, bit 1 is always 0, and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (if Memory space). Value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in LAS3RR register, only provides status to the system, and has no effect on operation of the PCI 9052. Associated Bus Region Descriptor Register (LAS3RR) controls prefetching features of this address space. (Specified in LAS3RR register.) If I/O space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Base Address. Base address for accesses to Local Address Space.	Yes	Yes	0

Note: *PCIBAR5 can be enabled or disabled by setting or clearing bit 0 in the LAS3BA register.*

Table 5-18. (PCICIS; 28h) PCI Cardbus CIS Pointer Register

Bit	Description	Read	Write	Value after Reset
31:0	Cardbus Information Structure Pointer for PCMCIA. **Not Supported.**	Yes	No	0

Table 5-19. (PCISVID; 2Ch) PCI Subsystem Vendor ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem Vendor ID. (Unique add-in board Vendor ID.)	Yes	Serial EEPROM	0

Table 5-20. (PCISID; 2Eh) PCI Subsystem ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem ID. (Unique add-in board Device ID.)	Yes	Serial EEPROM	0

Table 5-21. (PCIERBAR; 30h) PCI Expansion ROM Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Address Decode Enable. Value of 1 indicates the device accepts accesses to expansion ROM address. Value of 0 indicates the device does not accept accesses to expansion ROM space.	Yes	Yes	0
10:1	***Reserved***.	Yes	No	0
31:11	Expansion ROM Base Address (upper 21 bits).	Yes	Yes	0

Table 5-22. (PCIILR; 3Ch) PCI Interrupt Line Register

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Line Routing Value. Indicates to which system interrupt controller(s) input the interrupt line of device is connected.	Yes	Yes	0

Table 5-23. (PCIIPR; 3Dh) PCI Interrupt Pin Register

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Pin Register. Indicates interrupt pin device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD# ***Note:*** *The PCI 9052 supports only one PCI interrupt (INTA#).*	Yes	Serial EEPROM	1h

Table 5-24. (PCIMGR; 3Eh) PCI Min_Gnt Register

Bit	Description	Read	Write	Value after Reset
7:0	Min_Gnt. Specifies needed length of Burst period for the device, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments. **Not Supported.**	Yes	No	0

Table 5-25. (PCIMLR; 3Fh) PCI Max_Lat Register

Bit	Description	Read	Write	Value after Reset
7:0	Max_Lat. Specifies how often the device must gain access to the PCI bus. Value is a multiple of 1/4 µs increments. **Not Supported.**	Yes	No	0

5.3 Local Configuration Registers

Table 5-26. (LAS0RR; 00h) Local Address Space 0 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates Local Address Space 0 maps into PCI memory space. Value of 1 indicates Local Address Space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, value of 1 indicates that reads are prefetchable (Bit has no effect on operation of the PCI 9052, but is for system status.) If mapped into I/O space, bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to Local Bus Space 0. Each bit corresponds to an address bit. Bit 27 corresponds to Address bit 27. Value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration Register 18h). Default is 1 MB.	Yes	Yes	FF0000
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 5-27. (LAS1RR; 04h) Local Address Space 1 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates Local Address Space 1 maps into PCI memory space. Value of 1 indicates Local Address Space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, value of 1 indicates that reads are prefetchable. If mapped into I/O space, the bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to Local Bus Space 1. Each bit corresponds to an address bit. Bit 27 corresponds to Address bit 27. Value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration register 1Ch).	Yes	Yes	0
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 5-28. (LAS2RR; 08h) Local Address Space 2 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates Local Address Space 2 maps into PCI memory space. Value of 1 indicates Local Address Space 2 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, value of 1 indicates that reads are prefetchable. If mapped into I/O space, the bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to Local Bus Space 2. Each bit corresponds to an address bit. Bit 27 corresponds to Address bit 27. Value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with Configuration register 20h).	Yes	Yes	0
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 5-29. (LAS3RR; 0Ch) Local Address Space 3 Range Register

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates to Local Address Space 3 maps into PCI memory space. Value of 1 indicates Local Address Space 3 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI address space 0 1 Locate below 1 MB in PCI address space 1 0 Locate anywhere in 64-bit PCI address space 1 1 ***Reserved*** If mapped into I/O space, bit 1 must be a value of 0. Bit 2 is included with bits [27:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into Memory space, value of 1 indicates that reads are prefetchable. If mapped into I/O space, the bit is included with bits [27:2] to indicate decoding range.	Yes	Yes	0
27:4	Specifies PCI address bits used to decode PCI access to Local Bus Space 3. Each bit corresponds to an address bit. Bit 27 corresponds to Address bit 27. Value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration register 24h).	Yes	Yes	0
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0

Table 5-30. (EROMRR; 10h) Expansion ROM Range Register

Bit	Description	Read	Write	Value after Reset
0	Address Decode Enable. Bit 0 can only be enabled from serial EEPROM. To disable, refer to (PCIERBAR; 30h [0]).	No	Serial EEPROM Only	0
10:1	Unused.	Yes	No	0
27:11	Specifies PCI address bits used to decode PCI to local bus expansion ROM. Each bit corresponds to an Address bit. Value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCI Configuration register 30h). Default is 64 KB.	Yes	Yes	11111111111100000
31:28	Unused. (PCI address bits [31:28] are always included in decoding.)	Yes	Yes	1111

Table 5-31. (LAS0BA; 14h) Local Address Space 0 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 0 Enable. Value of 1 enables decode of PCI addresses for Direct Slave access to Local Space 0. Value of 0 disables decode.	Yes	Yes	1
1	Unused.	Yes	Yes	0
3:2	If Local Space 0 is mapped into Memory space, these bits are not used. If mapped into I/O space, these bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 0 into a Local Address Space. The bits in this register remap (replace) PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0

Table 5-32. (LAS1BA; 18h) Local Address Space 1 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 1 Enable. Value of 1 enables decode of PCI addresses for Direct Slave access to Local Space 1. Value of 0 disables decode.	Yes	Yes	0
1	Unused.	Yes	Yes	0
3:2	If to Local Space 1 is mapped into Memory space, these bits are not used. If mapped into I/O space, these bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 1 into a Local Address Space. The bits in this register remap (replace) PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0

Table 5-33. (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 2 Enable. Value of 1 enables decode of PCI addresses for Direct Slave access to Local Space 2. Value of 0 disables decode.	Yes	Yes	0
1	Unused.	Yes	Yes	0
3:2	If Local Space 2 is mapped into Memory space, these bits are not used. If mapped into I/O space, these bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 2 into a Local Address Space. The bits in this register remap (replace) PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0

Table 5-34. (LAS3BA; 20h) Local Address Space 3 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 3 Enable. Value of 1 enables decode of PCI addresses for Direct Slave access to Local Space 3. Value of 0 disables decode.	Yes	Yes	0
1	Unused.	Yes	Yes	0
3:2	If Local Space 3 is mapped into Memory space, these bits are not used. If mapped into I/O space, these bits are included with bits [27:4] for remapping.	Yes	Yes	0
27:4	Remap of PCI Address to Local Address Space 3 into a Local Address Space. The bits in this register remap (replace) PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0

Table 5-35. (EROMBA; 24h) Expansion ROM Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
10:0	Unused.	Yes	No	0
27:11	Remap of PCI Expansion ROM space into a Local Address Space. The bits in this register remap (replace) PCI address bits used in decode as the local address bits. Default base is 1 MB (above default Local Address Space 0).	Yes	Yes	00000001000000000
31:28	Unused. (Local address bits [31:28] do not exist in the PCI 9052.)	Yes	No	0

Table 5-36. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting only occurs if Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. Value of 1 indicates READY input enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. Value of 1 indicates Bterm Input is enabled. Value of 0 indicates Bterm Input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. Value of 1 prefetches up to the number of Lwords specified in prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8 bit 01 = 16 bit 10 = 32 bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until end of cycle (0-3).	Yes	Yes	0

Table 5-37. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting only occurs if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. Value of 1 indicates Bterm Input is enabled. Value of 0 indicates Bterm Input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. Value of 1 prefetches up to the number of Lwords specified in prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8 bit 01 = 16 bit 10 = 32 bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until end of cycle (0-3).	Yes	Yes	0

Table 5-38. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting only occurs if Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. Value of 1 indicates Bterm Input is enabled. Value of 0 indicates Bterm Input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. Value of 1 prefetches up to the number of Lwords specified in prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8 bit 01 = 16 bit 10 = 32 bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. 1 = Big Endian 0 = Little Endian	Yes	Yes	0
25	Big Endian Byte Lane Mode. Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until end of cycle (0-3).	Yes	Yes	0

Table 5-39. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting only occurs if Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. Value of 1 indicates Bterm Input is enabled. Value of 0 indicates Bterm Input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. Value of 1 prefetches up to the number of Lwords specified in prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8 bit 01 = 16 bit 10 = 32 bit 11 = ***Reserved***	Yes	Yes	10
24	Byte Ordering. Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until end of cycle (0-3).	Yes	Yes	0

Table 5-40. (EROMBRD; 38h) Expansion ROM Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Burst Enable. Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting only occurs if Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	Bterm Input Enable. Value of 1 indicates Bterm Input is enabled. Value of 0 indicates Bterm Input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	Prefetch Count. Number of Lwords to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable. Value of 1 prefetches up to the number of Lwords specified in prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width. 00 = 8 bit 01 = 16 bit 10 = 32 bit 11 = ***Reserved***	Yes	Yes	0
24	Byte Ordering. Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	Big Endian Byte Lane Mode. Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit local bus, and byte lane [31:24] for an 8-bit local bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit local bus, and byte lane [7:0] for an 8-bit local bus	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be ≤ NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be ≤ NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR de-assertion until end of cycle (0-3).	Yes	Yes	0

Table 5-41. (CS0BASE; 3Ch) Chip Select 0 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 0 Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 0. Write zeroes in the least significant bits to define the range for Chip Select 0. Starting from bit 1 and scanning toward bit 27, the first “1” found defines size. The remaining most significant bits, excluding the first “1” found, define base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 5-42. (CS1BASE; 40h) Chip Select 1 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 1 Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 1. Write zeroes in the least significant bits to define the range for Chip Select 1. Starting from bit 1 and scanning toward bit 27, the first “1” found defines size. The remaining most significant bits, excluding the first “1” found, define base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 5-43. (CS2BASE; 44h) Chip Select 2 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 2 Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 2. Write zeroes in the least significant bits to define the range for Chip Select 2. Starting from bit 1 and scanning toward bit 27, the first “1” found defines size. The remaining most significant bits, excluding the first “1” found, define the base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 5-44. (CS3BASE; 48h) Chip Select 3 Base Address Register

Bit	Description	Read	Write	Value after Reset
0	Chip Select 3 Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	Local Base Address of Chip Select 3. Write zeroes in the least significant bits to define the range for Chip Select 3. Starting from bit 1 and scanning toward bit 27, the first “1” found defines size. The remaining most significant bits, excluding the first “1” found, define base address.	Yes	Yes	0
31:28	Unused.	Yes	No	0

Table 5-45. (INTCSR; 4Ch) Interrupt Control/Status Register

Bit	Description	Read	Write	Value after Reset
0	Local Interrupt 1 Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
1	Local Interrupt 1 Polarity. Value of 1 indicates Active high. Value of 0 indicates Active low.	Yes	Yes	0
2	Local Interrupt 1 Status. Value of 1 indicates Interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
3	Local Interrupt 2 Enable. Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
4	Local Interrupt 2 Polarity. Value of 1 indicates Active high. Value of 0 indicates Active low.	Yes	Yes	0
5	Local Interrupt 2 Status. Value of 1 indicates Interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
6	PCI Interrupt Enable. Value of 1 enables PCI interrupt.	Yes	Yes	0
7	Software Interrupt. Value of 1 generates interrupt.	Yes	Yes	0
8	Local Interrupt 1 Select Enable. Value of 1 indicates enabled edge triggerable interrupt. Value of 0 indicates enabled level triggerable interrupt. ***Note:*** *Operates only in high polarity mode.*	Yes	Yes	0
9	Local Interrupt 2 Select Enable. Value of 2 indicates enabled edge triggerable interrupt. Value of 0 indicates enabled level triggerable interrupt. ***Note:*** *Operates only in high polarity mode.*	Yes	Yes	0
10	Local Edge Triggerable Interrupt Clear Bit. Writing 1 to this bit clears Interrupt_1.	Yes	Yes	0
11	Local Edge Triggerable Interrupt Clear Bit. Writing 2 to this bit clears Interrupt_2.	Yes	Yes	0
12	ISA Interface Mode Enable. Writing 1 enables ISA Interface mode. Writing 0 disables ISA Interface mode.	Yes	Serial EEPROM only	0
31:13	Unused.	Yes	No	0

Table 5-46. (CNTRL; 50h) User I/O, PCI Target Response, Serial EEPROM, Initialization Control Register

Bit	Description	Read	Write	Value after Reset
0	User I/O 0 or WAITO# Pin Select. Selects the function of USER0/WAITO# pin. Value of 1 indicates pin is WAITO#. Value of 0 indicates pin is USER0.	Yes	Yes	0
1	User I/O 0 Direction. Value of 0 indicates Input. Value of 1 indicates Output. Always an output if WAITO# function is selected.	Yes	Yes	0
2	User I/O 0 Data. If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
3	User I/O 1 or LLOCKo# Pin Select. Selects the function of USER1/LLOCKo# pin. Value of 1 indicates pin is LLOCKo#. Value of 0 indicates pin is USER1.	Yes	Yes	0
4	User I/O 1 Direction. Value of 0 indicates Input. Value of 1 indicates Output. Always an output if LLOCK function is selected.	Yes	Yes	0
5	User I/O 1 Data. If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
6	User I/O 2 or CS2# Pin Select. Selects the function of USER2/CS2# pin. Value of 1 indicates pin is CS2#. Value of 0 indicates pin is USER2.	Yes	Yes	0
7	User I/O 2 Direction. Value of 0 indicates Input. Value of 1 indicates Output. Always an output if CS2 function is selected.	Yes	Yes	0
8	User I/O 2 Data. If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
9	User I/O 3 or CS3# Pin Select. Selects the function of USER3/CS3# pin. Value of 1 indicates pin is CS3#. Value of 0 indicates pin is USER3.	Yes	Yes	0
10	User I/O 3 Direction. Value of 0 indicates Input. Value of 1 indicates Output. Always an output if CS3 function is selected.	Yes	Yes	0
11	User I/O 3 Data. If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
13:12	PCI Configuration Base Address Register (PCIBAR) Enables. 00 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled. 01 = PCIBAR0 (Memory) only. 10 = PCIBAR1 (I/O) only. 11 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled.	Yes	Yes	00
14	PCI Read Mode. Value of 1 immediately disconnects for a read. Prefetch the data into the direct slave read FIFO. Returns data when PCI read cycle is reapplied (PCI Specification v2.1 compatible). Value of 0 de-asserts TRDY# until read data is available.	Yes	Yes	0
15	PCI Read with Write Flush Mode. Value of 1 flushes pending read cycle if write cycle is detected. Value of 0 does not affect pending reads when a write cycle occurs (PCI Specification v2.1 compatible).	Yes	Yes	0
16	PCI Read No Flush Mode. Value of 1 does not flush the read FIFO if a PCI read cycle completes (Read Ahead mode). Value of 0 flushes the read FIFO if a PCI read cycle completes.	Yes	Yes	0
17	PCI Read No Write Mode. Value of 1 forces retry on writes if read is pending. Value of 0 allows a write to occur while a read is pending.	Yes	Yes	0
18	PCI Write Mode. Value of 1 disconnects if the write FIFO becomes full. Value of 0 de-asserts TRDY# until space is available in the direct slave write FIFO.	Yes	Yes	0

Table 5-46. (CNTRL; 50h) User I/O, PCI Target Response, Serial EEPROM, Initialization Control Register (continued)

Bit	Description	Read	Write	Value after Reset
22:19	PCI Target Retry Delay Clocks. Number of PCI clocks (multiplied by 8) after the beginning of a direct slave cycle until a retry is issued. Only valid for read cycles if bit 14 is low. Only valid for write cycles if bit 17 is low.	Yes	Yes	4
23	Direct Slave Lock Enable. Value of 1 enables PCI direct slave locked sequences. Value of 0 disables direct slave locked sequences.	Yes	Yes	0
24	Serial EEPROM Clock for Local or PCI Bus Reads or Writes to Serial EEPROM. Toggling this bit generates a serial EEPROM clock. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.)	Yes	Yes	0
25	Serial EEPROM Chip Select. For local or PCI bus reads or writes to serial EEPROM, setting this bit to 1 provides serial EEPROM chip select.	Yes	Yes	0
26	Write Bit to Serial EEPROM. For writes, this output bit is the input to serial EEPROM. Clocked into the serial EEPROM by serial EEPROM clock.	Yes	Yes	0
27	Read Serial EEPROM Data Bit. For reads, this input bit is the output of serial EEPROM. Clocked out of the serial EEPROM by serial EEPROM clock.	Yes	No	—
28	Serial EEPROM Valid. Value of 1 indicates a valid serial EEPROM is present.	Yes	No	0
29	Reload Configuration Registers. When set to 0, writing a value of 1 causes the PCI 9052 to reload the local configuration registers from serial EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. Value of 1 resets the PCI 9052 and issues a reset to the local bus. The PCI and local configuration register contents will not be reset.	Yes	Yes	0
31	Mask Revision.	Yes	No	0

6. PIN DESCRIPTION

6.1 Pin Summary

Table 6-2 through Table 6-5 describe the PCI 9052 pins:

- Power and ground
- Serial EEPROM interface
- PCI system bus interface
- Local bus support

Table 6-6 through Table 6-8 describe the local bus data transfer pins:

- Mode independent
- Non-Multiplexed mode
- Multiplexed mode

Table 6-9 and Table 6-10 describe ISA-related pins.

Unspecified pins are no connects (NC).

The BTERM#, LRDYi#, and NOWS# pins have an 80k ohm internal pull-up resistor on the local side. The TEST pin has a 50k ohm internal pull-down resistor on the local side.

For a visual view of the chip pin layout, refer to Section 8.3, "PCI 9052 Pin Out."

Table 6-1 lists abbreviations used in this section to represent the various pin types.

Table 6-1. Pin Type Abbreviations

Abbreviation	Pin Type
I/O	Input and output pin
I	Input pin only
O	Output pin only
TS	Tri-state pin
OC	Open collector pin
TP	Totem pole pin
STS	Sustained tri-state pin, driven high for one CLK before float

Table 6-2. Power and Ground Pin Description (23 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
TEST	Test	1	I	99	Test pin. Pull high for test. Pull low for normal operation. When TEST is pulled high, all outputs except RD# (pin 126) are placed in tri-state. RD# provides a NANDTREE output when TEST is pulled high.
NC	Spare	2	N/A	45, 67	Unused.
VDD	Power	10	I	1, 10, 27, 41, 50, 66, 81, 103, 121, 146	Power supply pins (5 V). Liberal .01 to .1 µF decoupling capacitors should be placed near the PCI 9052.
VSS	Ground	10	I	9, 26, 40, 51, 65, 80, 104, 120, 147, 160	Ground pins.

Table 6-3. Serial EEPROM Interface Pin Description (4 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
EECS	Serial EEPROM Chip Select	1	O TP 6 mA	142	Serial EEPROM Chip Select.
EEDO	Serial EEPROM Data Out	1	I	143	Serial EEPROM Read Data.
EEDI	Serial EEPROM Data In	1	O TP 6 mA	145	Serial EEPROM Write Data.
EESK	Serial EEPROM Serial Data Clock	1	O TP 6 mA	144	Serial EEPROM Clock.

Table 6-4. PCI System Bus Interface Pin Description (49 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS 6 mA	150-157, 2-8, 11, 23-25, 28-32, 34-39, 42-43	Multiplexed on the same PCI pins. A bus transaction consists of an address phase, followed by one or more data phases. The PCI 9052 supports both read and write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I	158, 12, 22, 33	Multiplexed on the same PCI pins. During the address phase of a transaction, defines bus command. During data phase, used as Byte Enables. For additional information, refer to PCI Specification v2.1.
CLK	Clock	1	I	149	Provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33 MHz.
DEVSEL#	Device Select	1	O STS 6 mA	16	When actively driven, indicates the driving device has decoded its address as the target of current access.
FRAME#	Cycle Frame	1	I	13	Driven by the current master to indicate beginning and duration of an access. Asserted to indicate a bus transaction is beginning. While asserted, data transfers continue. When de-asserted, the transaction is in the final data phase.
IDSEL	Initialization Device Select	1	I	159	Chip select used during configuration read and write transactions.
INTA#	Interrupt A	1	O OC 6 mA	44	Requests an interrupt.
IRDY#	Initiator Ready	1	I	14	Indicates the ability of initiating agent (bus master) to complete current data phase of transaction.
LOCK#	Lock	1	I	18	Indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS 6 mA	21	Indicates even parity across AD[31:0] and C/BE[3:0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after address phase. For data phases, PAR is stable and valid one clock after IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after completion of current data phase.
PERR#	Parity Error	1	O STS 6 mA	19	Indicates only the reporting of data parity errors during all PCI transactions, except during a Special Cycle.
RST#	Reset	1	I	148	Brings PCI-specific registers, sequencers, and signals to a consistent state.
SERR#	Systems Error	1	O OC 6 mA	20	For reporting address parity errors, data parity errors on Special Cycle command, or any other system error where the result will be catastrophic.
STOP#	Stop	1	O STS 6 mA	17	Indicates the current target is requesting the master to stop the current transaction.
TRDY#	Target Ready	1	O STS 6 mA	15	Indicates the ability of target agent (selected device) to complete the current data phase of transaction.

Table 6-5. Local Bus Support Pin Descriptions (14 Pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
MODE	Bus Mode	1	I	68	Selects bus operation mode of the PCI 9052. 1 = Multiplexed Bus mode 0 = Non-Multiplexed mode
LINTi1	Local Interrupt 1 In	1	I	137	When asserted, causes a PCI interrupt. Polarity is determined by INTCSR configuration register.
LINTi2	Local Interrupt 2 In	1	I	136	When asserted, causes a PCI interrupt. Polarity is determined by INTCSR configuration register.
LCLK	Local Bus Clock	1	I	135	Local clock up to 40 MHz, and may be asynchronous to PCI clock.
LHOLD	Hold Request	1	I	134	Asserted by a local bus master to request use of the local bus.
LHOLDA	Hold Acknowledge	1	O TP 6 mA	133	Asserted by the PCI 9052 to grant control of the local bus to a local bus master. When the PCI 9052 needs the local bus, it signals a preempt by de-asserting LHOLDA.
LRESET#	Local Reset Out	1	O TP 6 MA	132	Local bus reset output, asserted when the PCI 9052 is reset, and used to reset devices on the local bus.
BCLKO	BCLK Out	1	O TP 24 mA	63	Indicates a buffered version of the PCI clock for optional use by the local bus.
CS[1:0]#	Chip Selects	2	O TS 6 mA	131, 130	General purpose chip selects. The base and range of each may be programmed in configuration registers.
USER0/WAITO#	User I/O 0 or WAIT Out	1	I/O TS 6 mA	138	Can be programmed to be a configurable User I/O pin, USER0, or the local bus WAIT out pin. WAITO# is asserted when wait states are caused by the internal wait-state generator. Serves as an output to provide ready-out status.
USER1/LLOCKo#	User I/O 1 or LLOCK Out	1	I/O TS 6 mA	139	Can be programmed to be a configurable User I/O pin, USER1, or the local bus LLOCK out pin, LLOCKo#. LLOCKo# indicates an atomic operation that may require multiple transactions to complete and can be used by the local bus to lock resources.
USER2/CS2#	User I/O 2 or CS2 Out	1	I/O TS 6 mA	140	Can be programmed to be a configurable User I/O pin, USER1, or as Chip Select 2 output pin, CS2#.
USER3/CS3#	User I/O 3 or CS3 Out	1	I/O TS 6 mA	141	Can be programmed to be a configurable User I/O pin, USER3, or as Chip Select 3 output pin, CS3#.

Table 6-6. Local Bus Data Transfer Pins Description (Mode Independent) (7 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	O TS 12 mA	123	Indicates valid address and start of a new bus access. Asserted for the first clock of a bus access.
ALE	Address Latch Enable	1	O TS 6 mA	64	Asserted during the address phase and de-asserted before data phase.
LW/R	Write/Read	1	O TS 6 mA	127	Asserted high for writes and low for reads.
BLAST#	Burst Last	1	O TS 6 mA	124	Signal driven by the current local bus master to indicate last transfer in a bus access.
RD#	Read Strobe	1	O TS 12 mA	126	General purpose read strobe. The timing is controlled by current Bus Region Descriptor Register.
WR#	Write Strobe	1	O TS 12 mA	125	General purpose write strobe. The timing is controlled by current Bus Region Descriptor Register.
LRDYi#	Local Ready In	1	I	128	Local ready input indicates read data is on the local bus, or that write data is accepted. Used in conjunction with the programmable wait-state generator.

Table 6-7. Local Bus Data Transfer Pins Description (Non-Multiplexed Mode) (63 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I	129	If disabled through the PCI 9052 configuration registers, the PCI 9052 bursts up to four transactions, Lword transfer depends upon bus width and type. If enabled, the PCI 9052 continues to burst until Bterm input is asserted. Ready input which breaks up a burst cycle and causes another address cycle to occur. Also used in conjunction with the wait state generator.
LA[27:2]	Address Bus	26	O TS 6 mA	122, 119-105, 102-100, 98-92	Carries the upper 26 bits of the 28-bit physical address bus. Increments during bursts to indicate successive data cycles.
LAD[31:0]	Data Bus	32	I/O TS 6 mA	52-62, 69-79, 82-91	Carries 32-, 16-, or 8-bit data quantities, depending on bus width configuration. 8 bit = LAD[7:0] 16 bit = LAD[15:0] 32 bit = LAD[31:0]
LBE[3:0]#	Byte Enables	4	O TS 12 mA	46-49	Byte enables are encoded based on configured bus width: **32-Bit Bus** Four byte enables indicate which of the four bytes are active during a data cycle. • LBE3# Byte Enable 3 = LAD[31:24] • LBE2# Byte Enable 2 = LAD[23:16] • LBE1# Byte Enable 1 = LAD[15:8] • LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE[3,1:0]# are encoded to provide BHE#, LA1, and BLE#. • LBE3# Byte High Enable (BHE#) = LAD[15:8] • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0]. • LBE3# Unused • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)

Table 6-8. Local Bus Data Transfer Pins Description (Multiplexed Mode) (63 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I	129	If disabled through the PCI 9052 configuration registers, the PCI 9052 will burst up to four transactions, Lword transfer depends upon the bus width and type. If enabled, the PCI 9052 continues to burst until BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. Also used in conjunction with the wait state generator.
LA[27:2]	Address Bus	26	O TS 6 mA	122, 119-105, 102-100, 98-92	Carries the upper 26 bits of the 28-bit physical address bus. During bursts LA[27:2] increments to indicate successive data cycles.
LAD[31:0]	Address/Data Bus	32	I/O TS 6 mA	52-62, 69-79, 82-91	During the address phase, bus carries the upper 26 bits of the 28-bit physical address bus. During the data phase, bus carries 32-, 16-, or 8-bit data quantities, depending on bus width configuration. 8 bit = LAD[7:0] 16 bit = LAD[15:0] 32 bit = LAD[31:0]
LBE[3:0]#	Byte Enables	4	O TS 12 mA	46-49	Byte enables are encoded based upon configured bus width: **32-Bit Bus** Four byte enables indicate which of the four bytes are active during a data cycle. • LBE3# Byte Enable 3 = LAD[31:24] • LBE2# Byte Enable 2 = LAD[23:16] • LBE1# Byte Enable 1 = LAD[15:8] • LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE[3,1:0]# are encoded to provide BHE#, LA1, and BLE#. • LBE3# Byte High Enable (BHE#) = LAD[15:8] • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0]. • LBE3# Unused • LBE2# Unused • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)

Table 6-9. ISA Local Bus Data Transfer Pins Description (Non-Multiplexed Mode)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
MEMWR#	Memory Write	1	O TS 6 mA	131	Command given to a memory slave to latch data from the ISA data bus.
MEMRD#	Memory Read	1	O TS 6 mA	130	Command given to a memory slave to drive the data onto ISA data bus.
IOWR#	I/O Write	1	O TS 6 mA	139	Command given to an ISA I/O slave device to latch data from the ISA data bus.
IORD#	I/O Read	1	O TS 6 mA	138	Command given to an ISA I/O slave device to drive data onto the ISA data bus.
SBHE#	System Byte High Enable	1	O TS 12 mA	46	When asserted, indicates that a byte is being transferred on the upper byte [15:8] of data bus.
ISAA[1:0]	ISA Address Bus	2	O TS 12 mA	48, 49	ISAA[1:0] are the ISA bus address phase bits. Bits [1:0] should be used in conjunction with LA[23:2]. For a 16-bit ISA bus, ISAA0 is used as an LBE# signal. For an 8-bit ISA bus, ISAA0 is used as an address bit.
BALE	Bus Address Latch Enable	1	O TS 6 mA	64	Asserted to indicate that the address and SBHE# signal lines are valid.
CHRDY	Channel Ready	1	I	45	Input from the slave device to indicate that additional time (wait states) is required to complete cycle. Signal goes low when the slave device requires wait states.
NOWS#	No Wait States	1	I	67	Input from the slave device to indicate that current cycle can be shortened after the slave has decoded address and command signals. A 16-bit ISA memory or I/O cycle can be reduced by 2 CLKs. An 8-bit memory or I/O cycle can be reduced by 3 CLKs. CHRDY has precedence over NOWS#.
LA[23:2]	Address Bus	22	O TS 6 mA	116-105, 102-100, 98-92	Address bus carries the upper 22 bits of the 28-bit physical address bus.
LAD[15:0]	Data Bus	16	I/O TS 6 mA	74-79, 82-91	Data bus phase. Bus carries 16-bit data quantities when configured to be 16-bit wide.
LAD[7:0]	Data Bus	8	I/O TS 6 mA	84-91	Data bus phase. Bus carries 8-bit data quantities when configured to be 8-bit wide.

Table 6-10. Generic Local Bus Support Pin Descriptions When ISA_MODE Enabled (Non-Multiplexed Mode)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
MODE	Bus Mode	1	I	68	Select bus operation mode of the PCI 9052: 1 = Multiplexed bus 0 = Non-multiplexed bus
LINTi1	Local Interrupt 1	1	I	137	Level Triggered: When asserted causes a PCI interrupt. Polarity is determined by INTCSR configuration register. Edged Triggered: Only for Positive polarity. When asserted causes a PCI interrupt. To clear, refer to the INTCSR configuration register.
LINTi2	Local Interrupt 2	1	I	136	Level Triggered: When asserted causes a PCI interrupt. Polarity is determined by INTCSR configuration register. Edged Triggered: Only for Positive polarity. When asserted causes a PCI interrupt. To clear, refer to the INTCSR configuration register.
LCLK	Local Bus Clock	1	I	135	Local clock for ISA 8 MHz, and may be asynchronous to the PCI clock.
LHOLD	Hold Request	1	I	134	A local bus master asserts LHOLD to request use of the Local Bus.
LHOLDA	Hold Acknowledge	1	O TP 6 mA	133	The PCI 9052 asserts LHOLDA to grant control of the local bus to a local bus master. When the PCI needs the local bus, it can signal a preempt by de-asserting.
LRESET	Local Reset Out	1	O TP 6 mA	132	Local Reset Out. When the ISA_MODE bit is enabled, the signal is active high. It is asserted when the PCI 9052 chip is reset, and used to reset devices on the local bus. ***Note:*** *LRESET is inverted if ISA mode is enabled.*
BCLKO	BCLK Out	1	O TP 24 mA	63	This is a buffered version of the PCI clock for optional use by the local bus.
USER2/CS2#	User I/O 2 or CS2 Out	1	I/O TS 6 mA	140	This pin can be programmed to be a configurable User I/O pin, or as the Chip Select 2 pin.
USER3/CS3#	User I/O 3 or CS3 Out	1	I/O TS 6 mA	141	This pin can be programmed to be a configurable User I/O pin, or as the Chip Select 3 pin.

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7. ELECTRICAL AND TIMING SPECIFICATIONS

7.1 General Specifications

Table 7-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage temperature	-65 to +150 °C
Ambient temperature with power applied	-55 to +125 °C
Supply voltage to ground	-0.5 to +7.0 V
Input voltage (VIN)	VSS -0.5 V VDD +0.5 V
Output voltage (VOUT)	VSS -0.5 V VDD +0.5 V

Table 7-2. Operating Ranges

Ambient Temperature	Junction Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0 to +70 °C	115 °C Maximum	5 V ±5%	Min = VSS Max = VDD

Table 7-3. Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN = 2.0 V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0 V f = 1 MHz	Output	10	pF

Table 7-4. Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min,	IOH = -4.0 mA	2.4	—	V
VOL	Output Low Voltage	VIN = VIH or VIL	IOL per Tables	—	0.4	V
VIH	Input High Level	—	—	2.0	—	V
VIL	Input Low Level	—	—	—	0.8	V
ILI	Input Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
IOZ	Tri-State Output Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
ICC	Power Supply Current	VDD = 5.25 V, PCLK = LCLK = 33 MHz		—	130	mA

7.2 Local Inputs

Local Bus Input Setup and Hold Times:

- Hold time = 2 ns min
- Setup time = 8 ns min

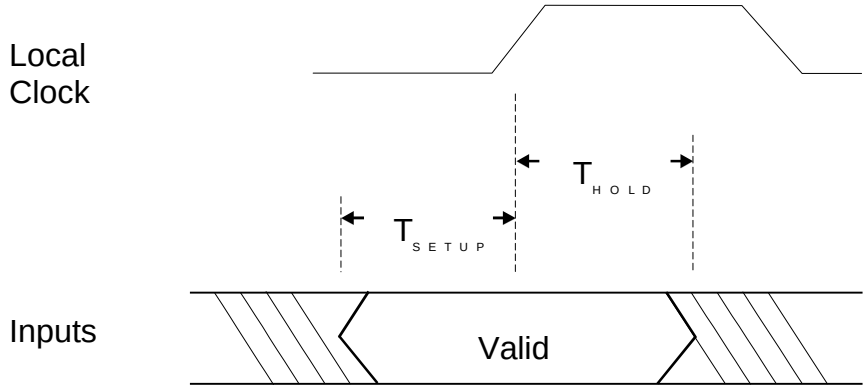

Figure 7-1. PCI 9052 Local Input Setup and Hold Waveform

Table 7-5. Clock Frequencies

Frequency	Min	Max
Local Clock Input	0	40 MHz
PCI Clock Input	0	33 MHz

7.3 Local Outputs

Table 7-6. AC Electrical Characteristics (Local Outputs) Measured over Operating Range

Signals (Synchronous Outputs) C_L = 50 pF, VCC = 5.0 ±5%	$T_{VALID\ (MIN)}$ NSEC	$T_{VALID\ (TYP)}$ NSEC	$T_{VALID\ (MAX)}$ NSEC (WORST CASE)
LHOLDA	3	—	9
ADS#	3	7.40	10
BLAST#	5	9.4	16
LBE[3:0]#	4	8.4	15
LW/R#	4	7.8	12
LAD[31:0]	5	14.6	16
LA[27:2]	5	18.6	14
LRESET#	5*	14	17*
RD#	7	9	27
WR#	4	9	13
BCLKO	2	7	8
WAITO#	—	9.6	—
LLOCKo#	—	8	—
USER[3:0]	4*	5*	12*
CS[3:0]#	4	11	17

Note: *Values followed with an asterisk (*) are referenced from the PCI side.*

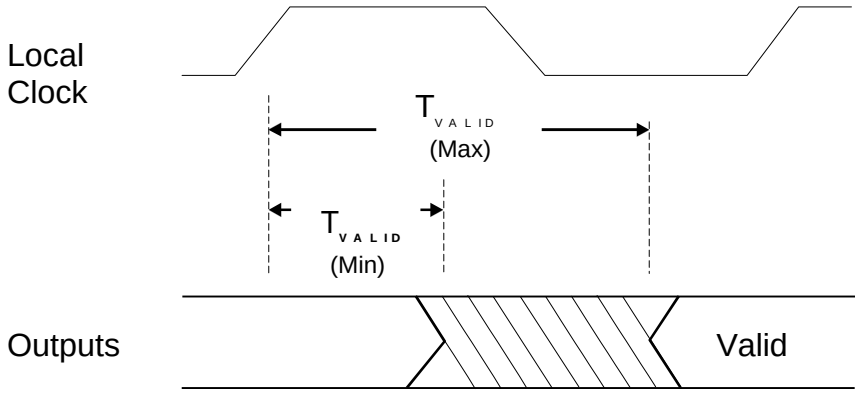

Figure 7-2. PCI 9052 Local Output Delay

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8. PACKAGE, SIGNAL, AND PIN OUT SPECS

8.1 Package Mechanical Dimensions

For 160-pin PQFP

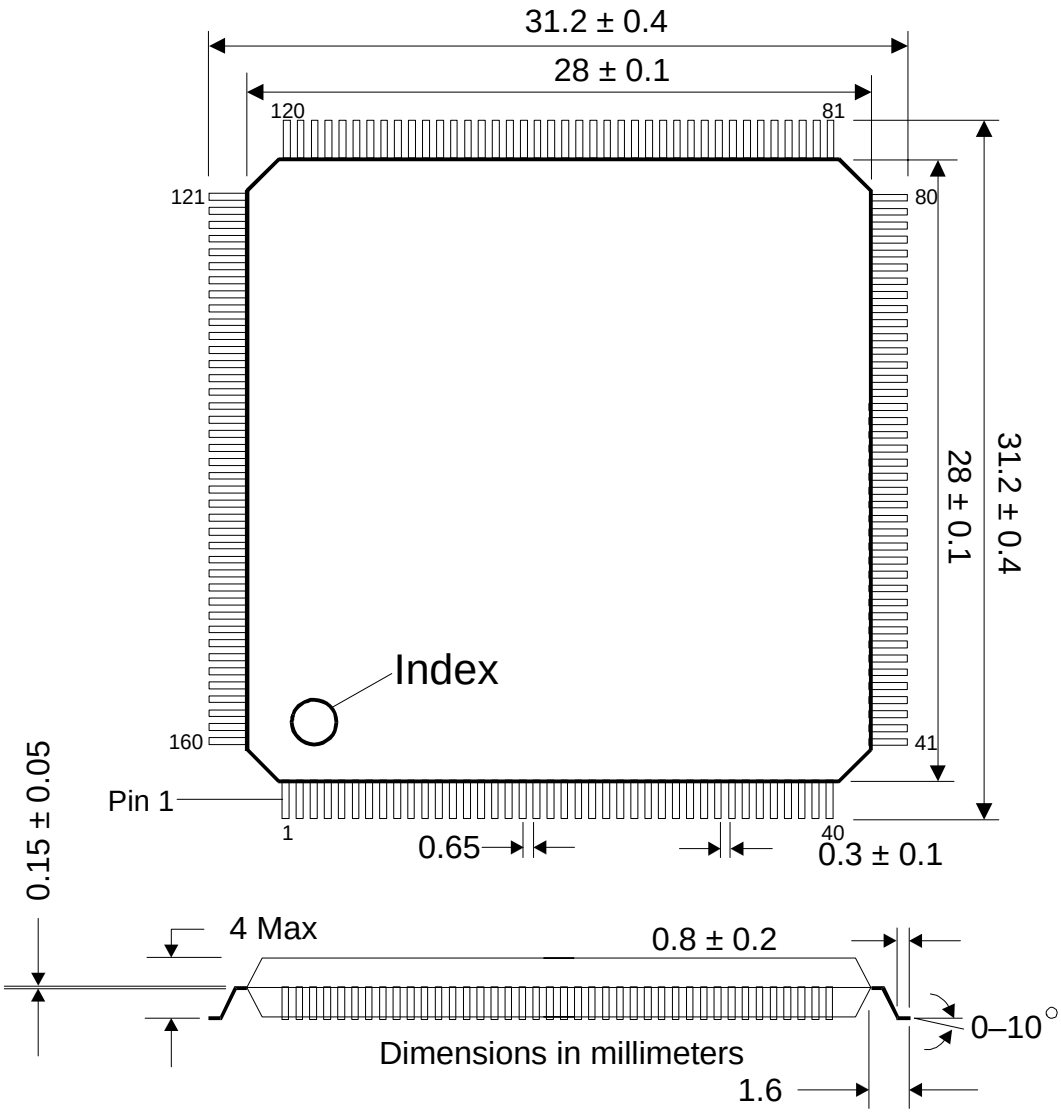


Figure 8-1. Package Mechanical Dimensions

8.2 Typical Bus Target Interface Adapter

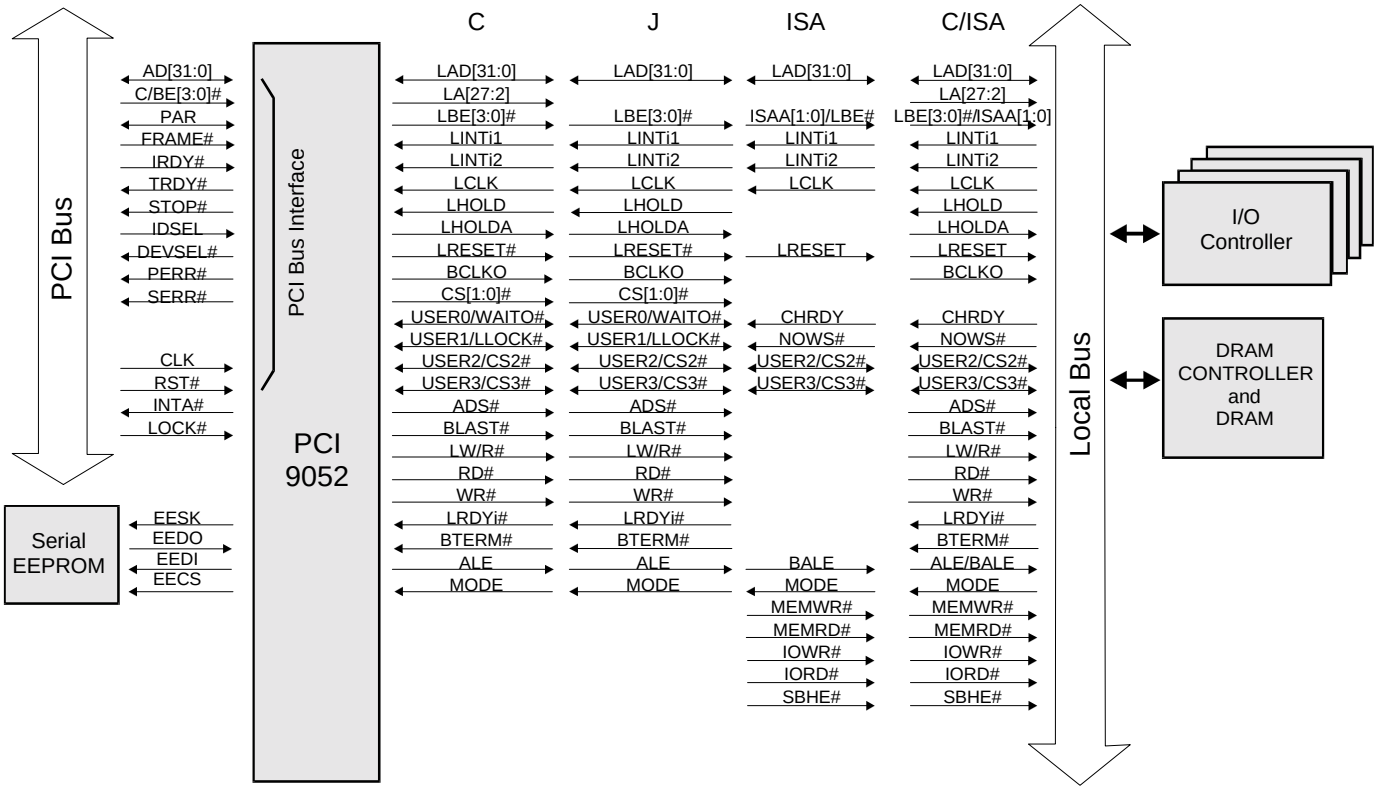


Figure 8-2. Typical Bus Target Interface Adapter (C, J, ISA, and C/ISA Modes)

8.3 PCI 9052 Pin Out

Refer to Section 6, “Pin Description,” for a complete description of each pin.

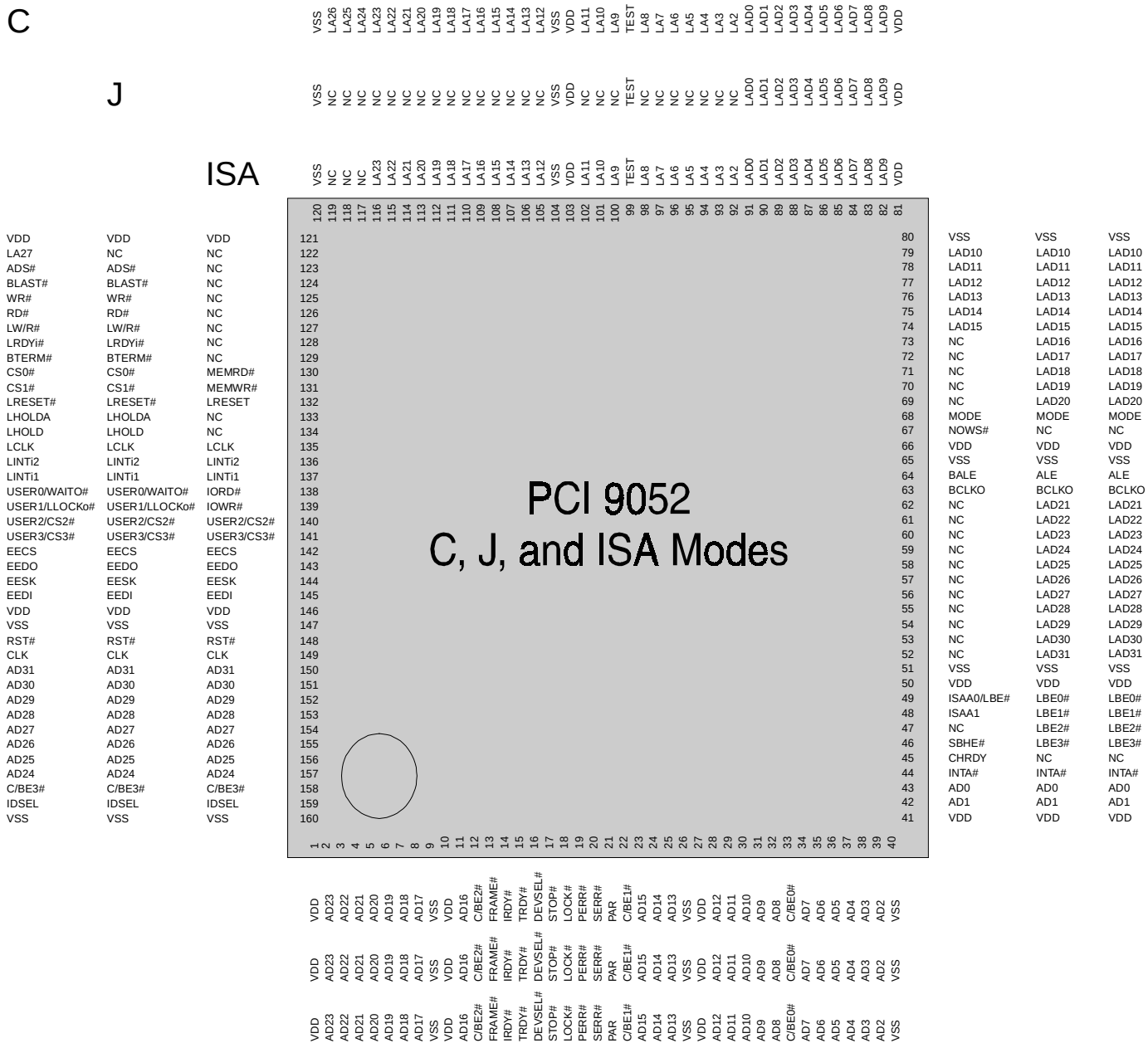


Figure 8-3. PCI 9052 Pin Out (C, J, and ISA Modes)

Note: *LRESET is inverted if ISA mode is enabled.*

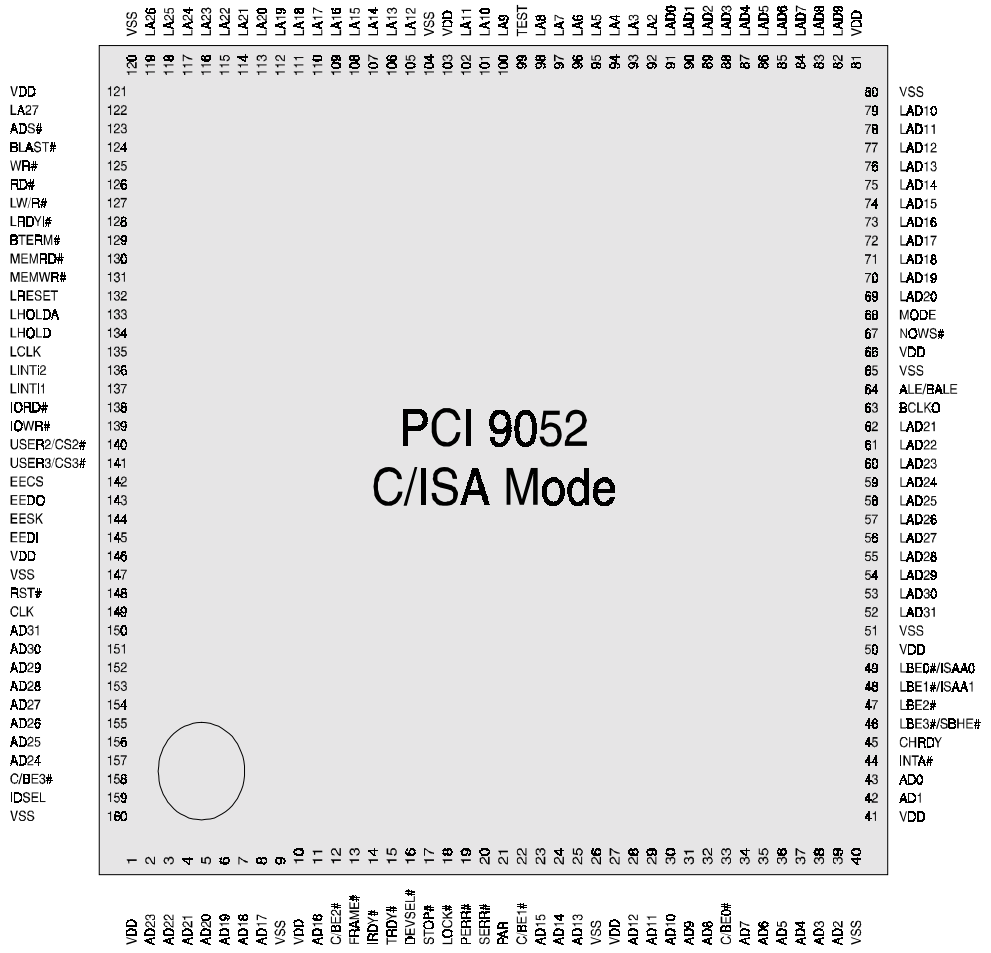


Figure 8-4. PCI 9052 Pin Out (C/ISA Mode)

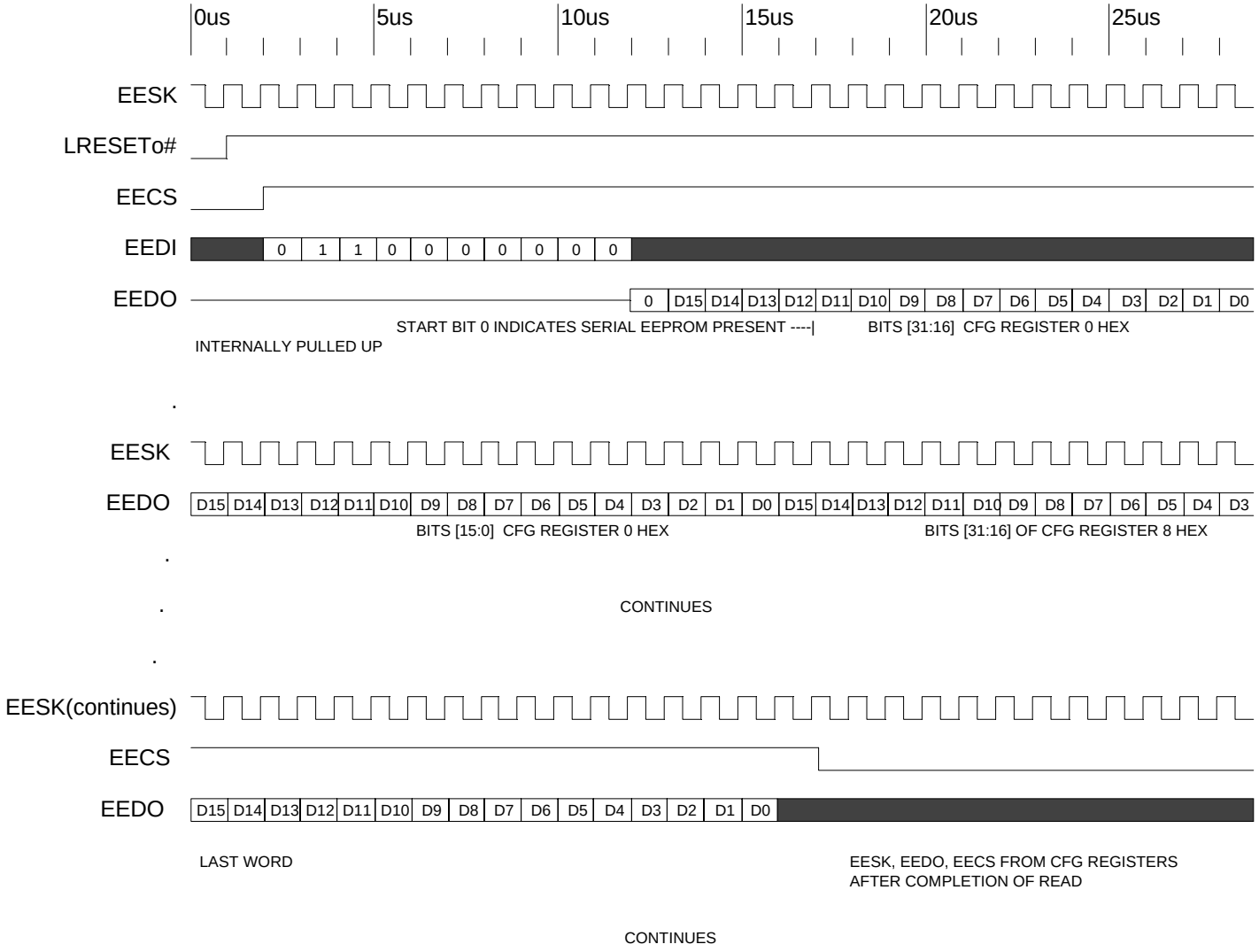
Note: *LRESET is inverted if ISA mode is enabled.*

9. TIMING DIAGRAMS

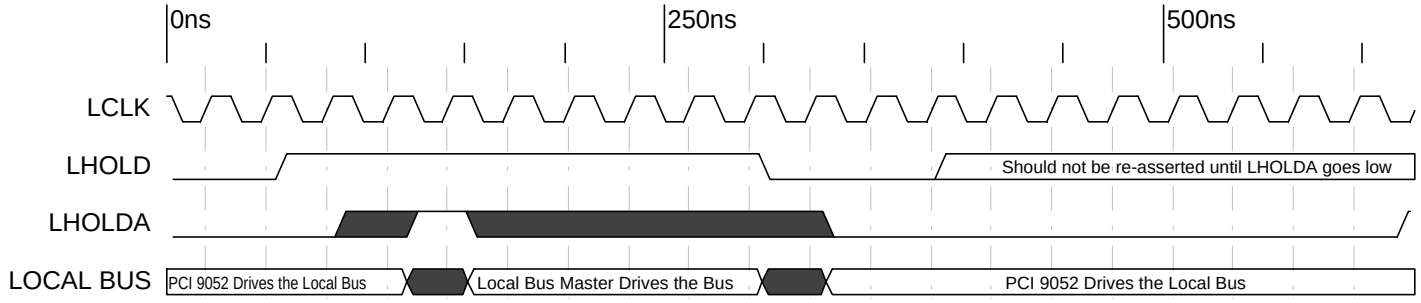
PCI 9052 operates in three modes, selected through mode pins, corresponding to three bus types—C, J, and ISA. Timing Diagrams are provided for the three operating modes. For some functions, a timing diagram may only be provided for one mode of operation. Although a different mode is used, the timing diagram can be used to determine functionality.

9.1 PCI/Local Timing Diagrams

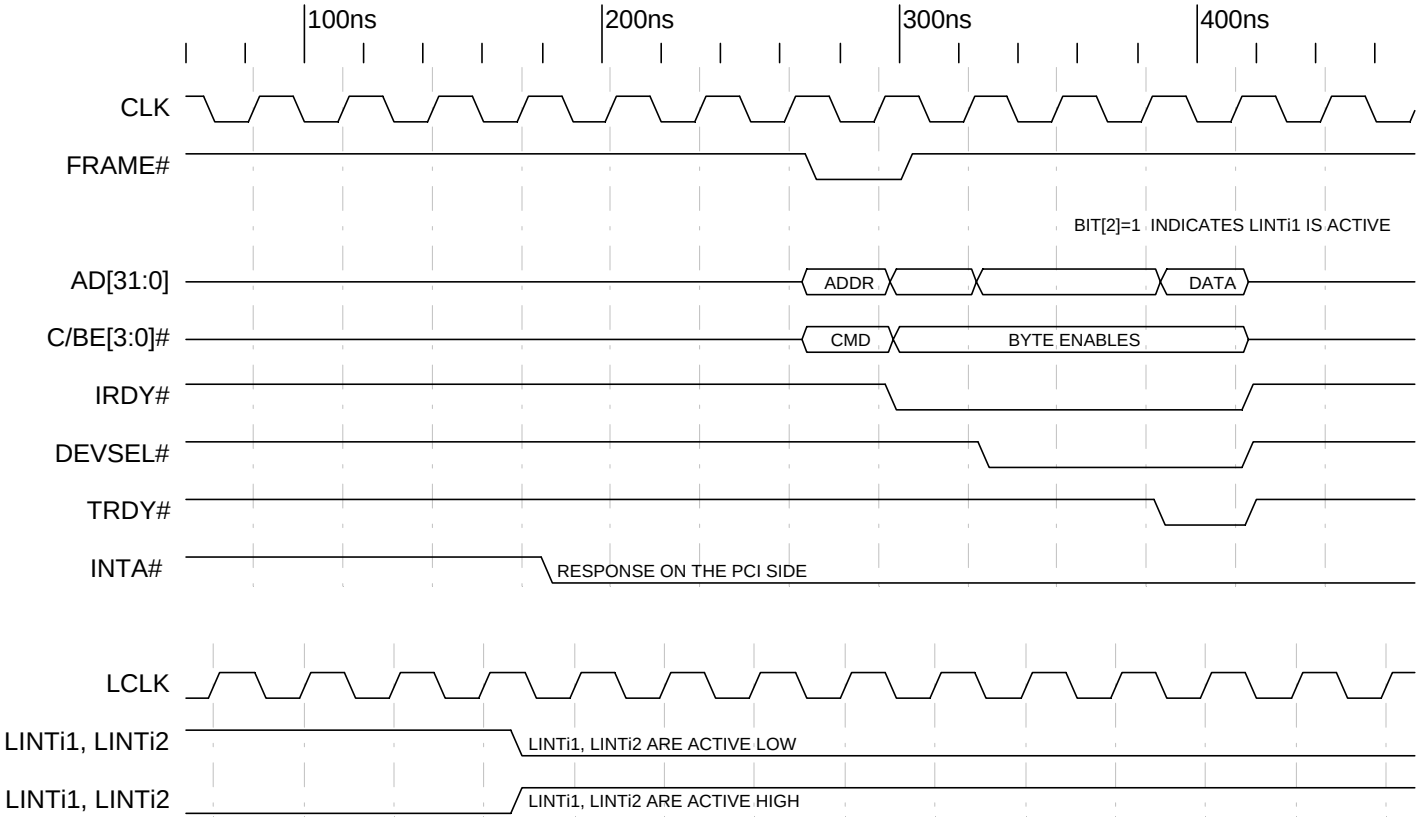
9.1.1 PCI 9052 Initialization



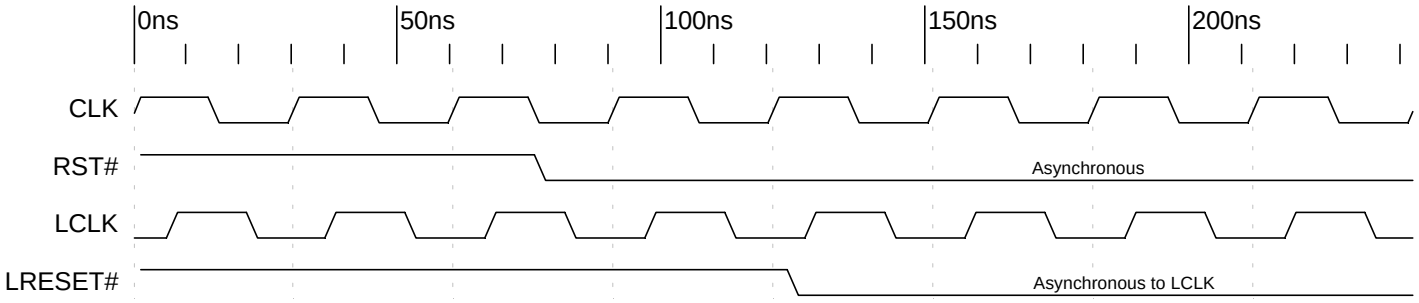
Timing Diagram 9-1. Initialization from Serial EEPROM



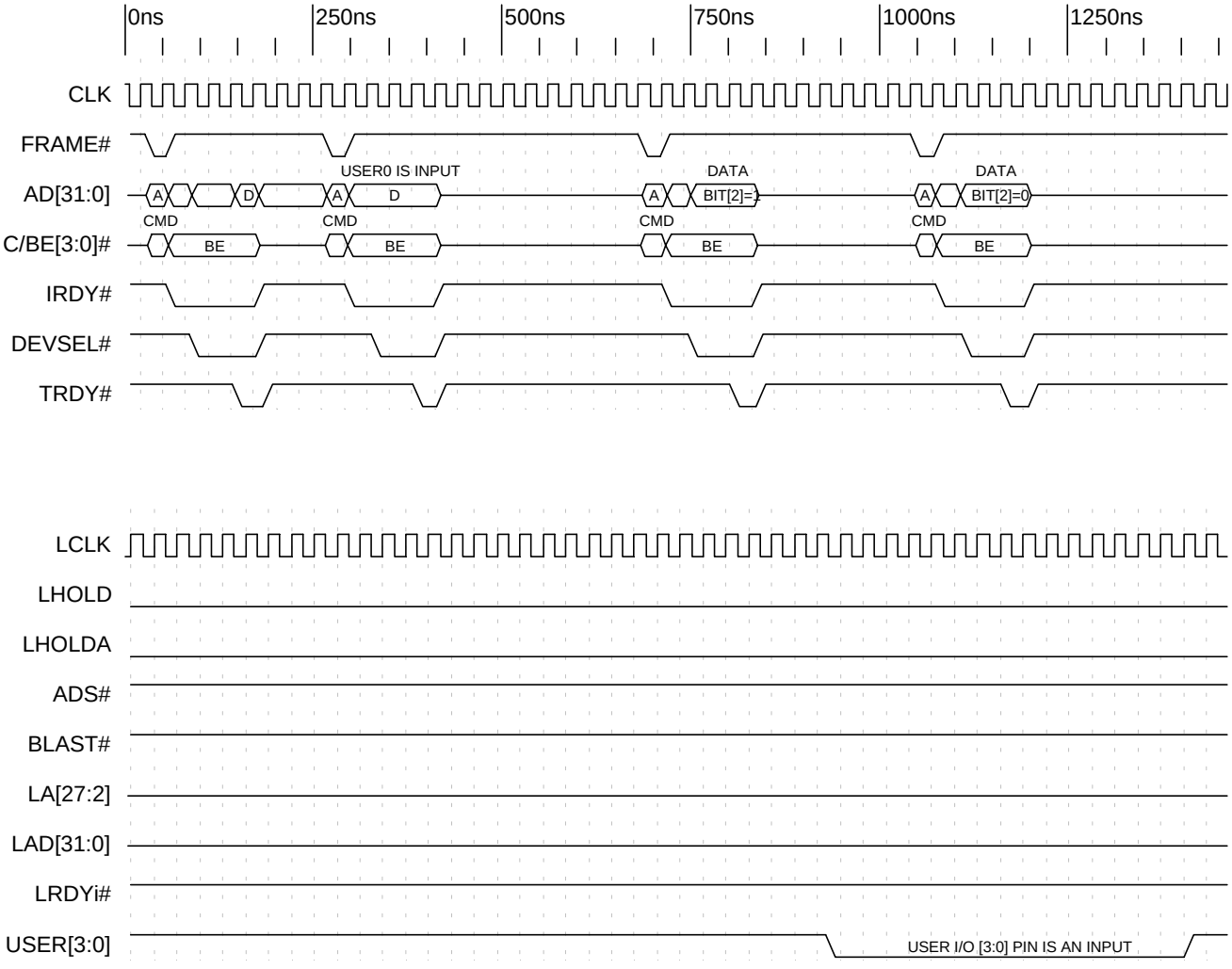
Timing Diagram 9-2. Local Bus Arbitration



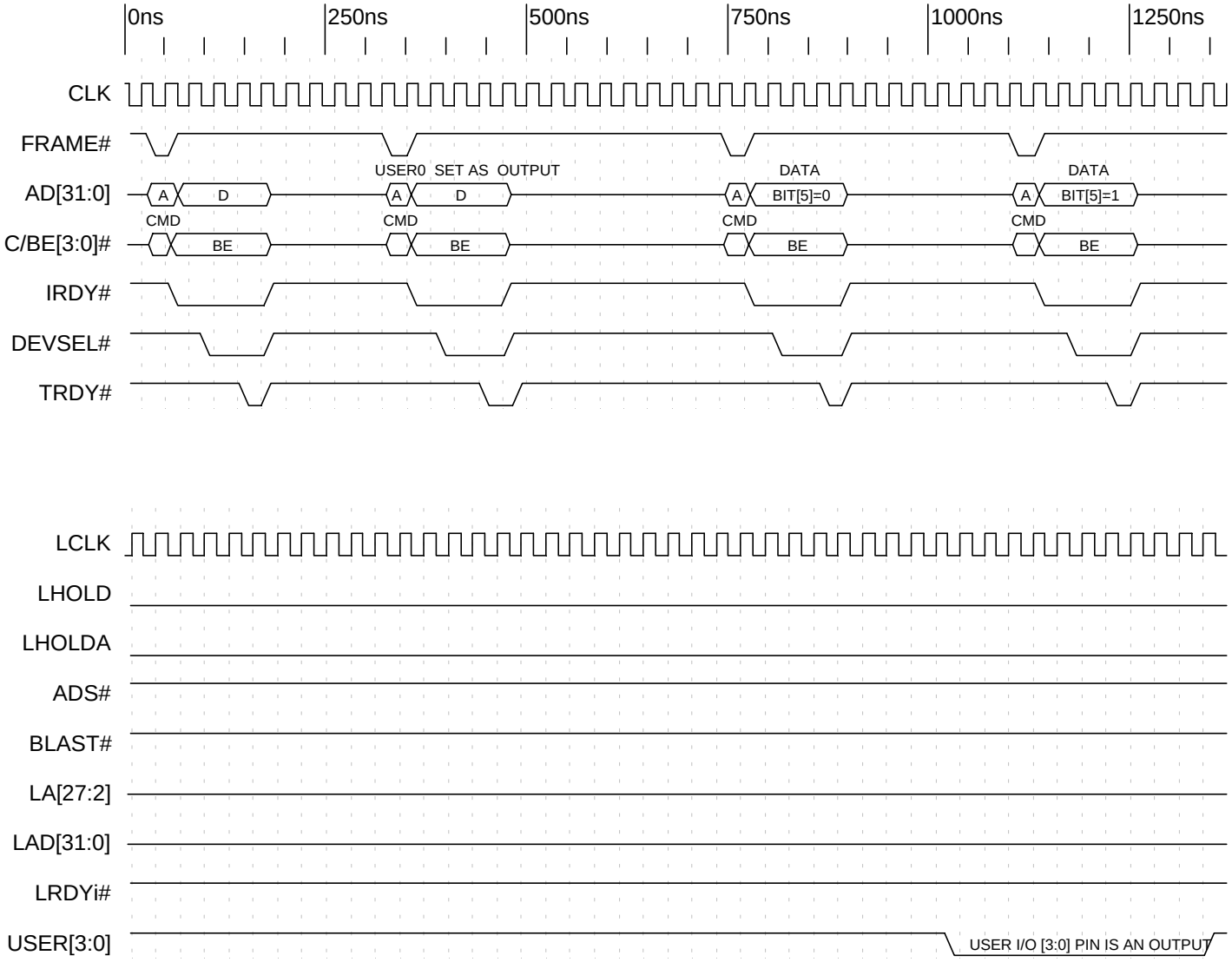
Timing Diagram 9-3. Local LINTi1 Input Asserting PCI Output INTA#



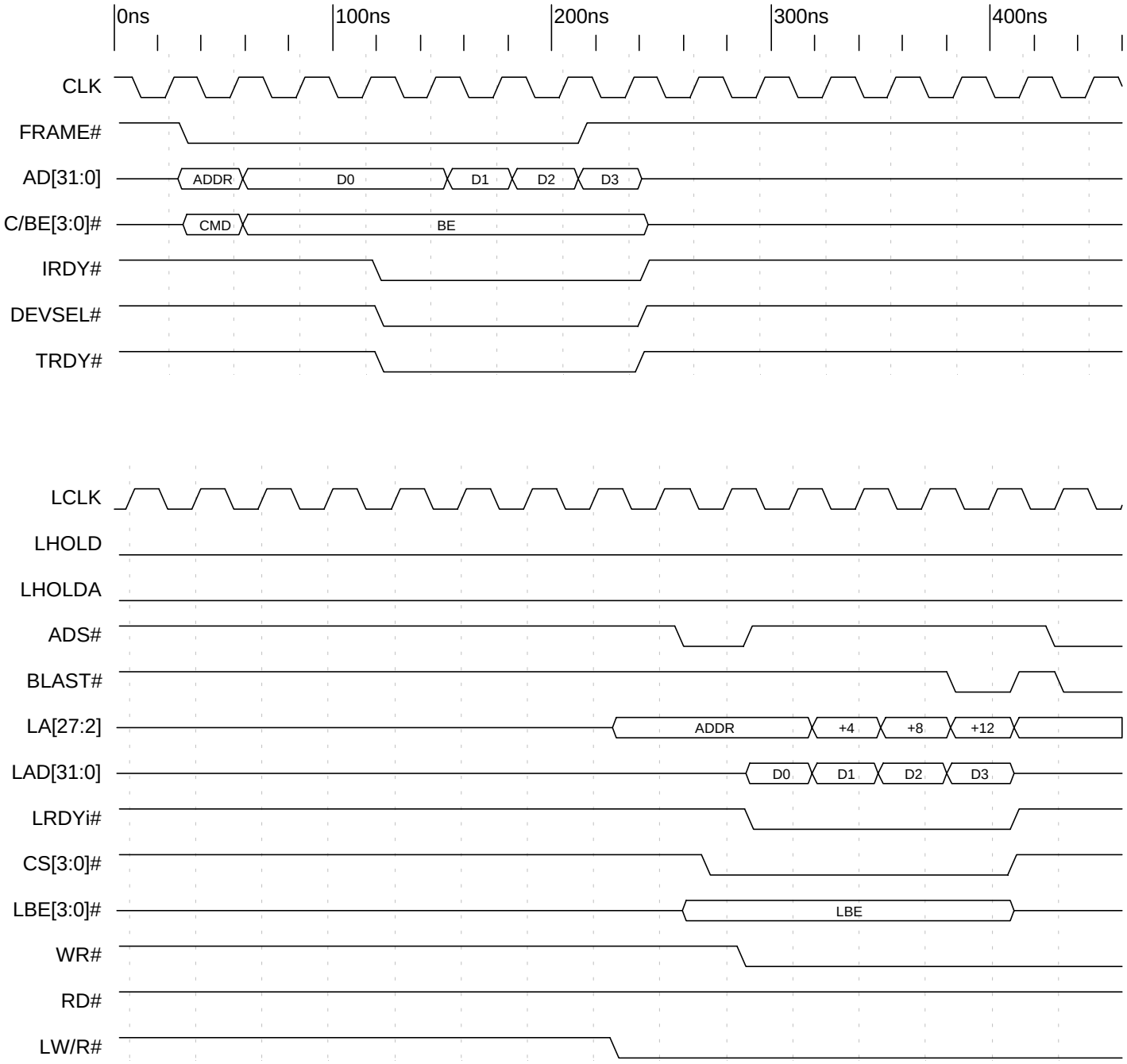
Timing Diagram 9-4. PCI RST# Asserting Local Output LRESET#



Timing Diagram 9-5. USER I/O Pin 0 Is an Input



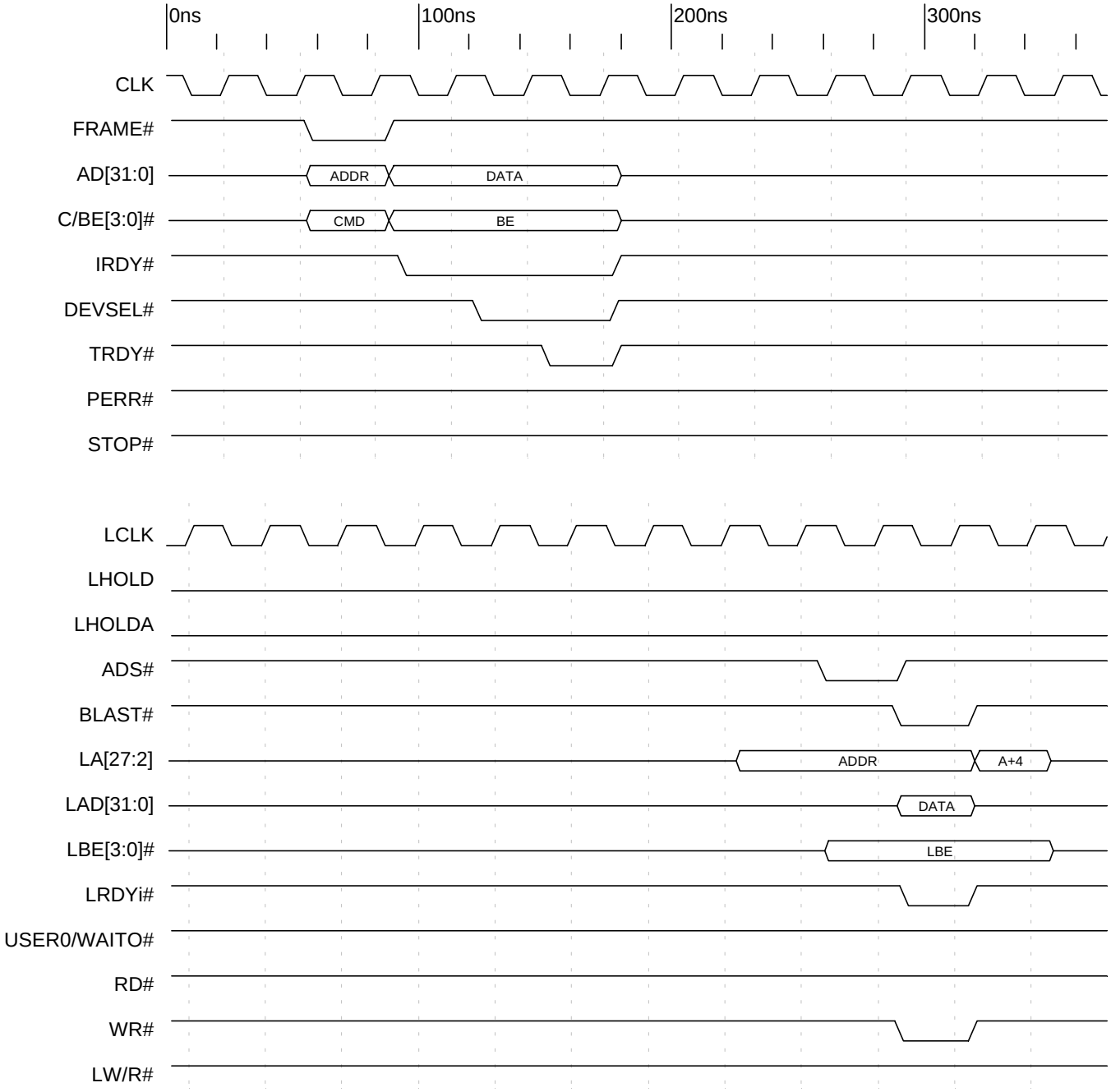
Timing Diagram 9-6. USER I/O Pin 0 Is an Output



CS0# Base Address is in the range of Space 0
CS0# is asserted same for the other chip selects

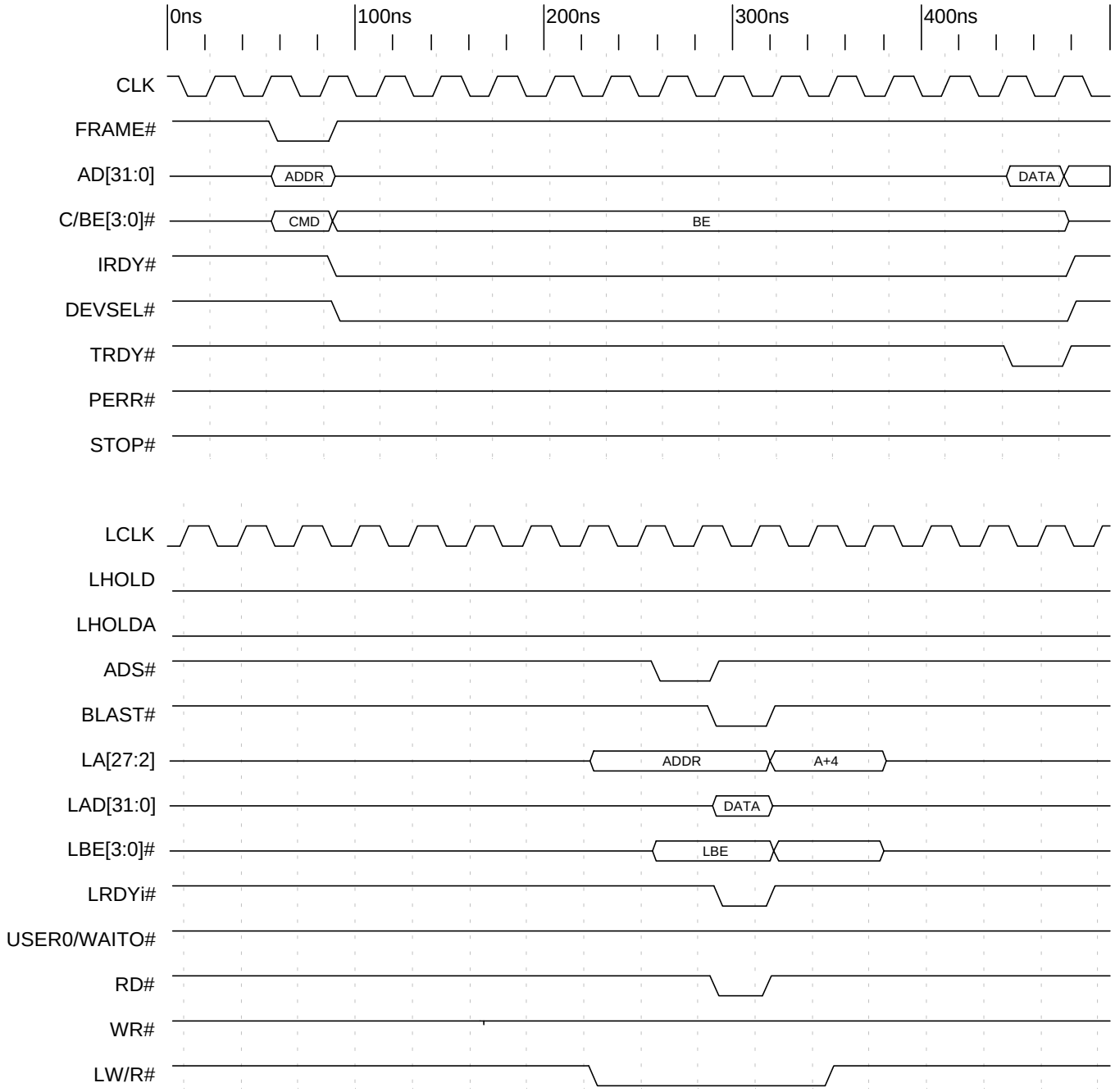
Timing Diagram 9-7. Chip Select 0

9.1.2 Direct Slave Single



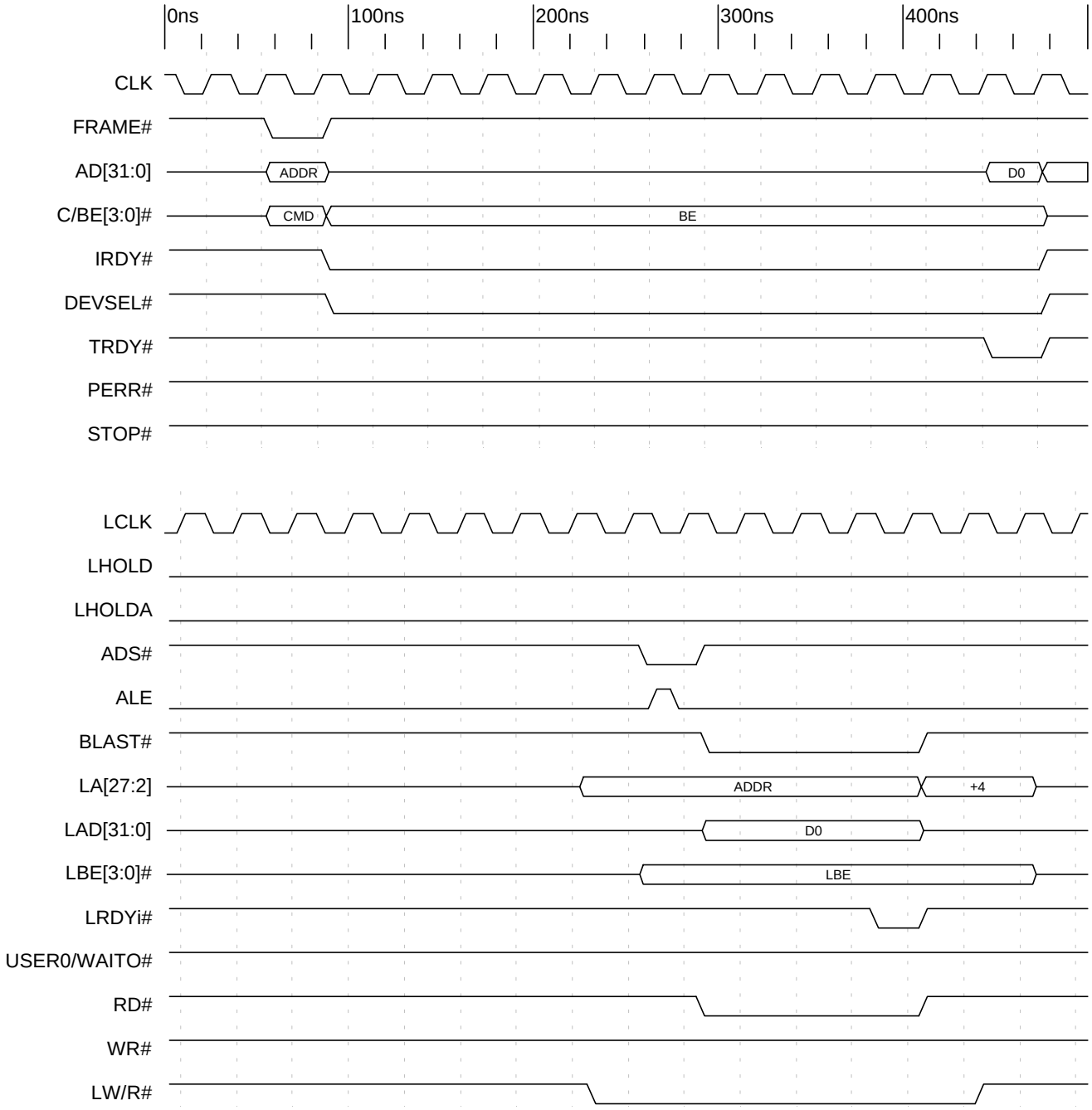
Single write, 32-bit local bus, without wait states
Space 0 is mapped to I/O
Address-to-data = zero wait state
Data-to-data = zero wait state
Read strobe = zero wait state

Timing Diagram 9-8. Direct Slave Single Write (32-Bit Local Bus)



Single read, 32-bit local bus, without wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe = zero wait states

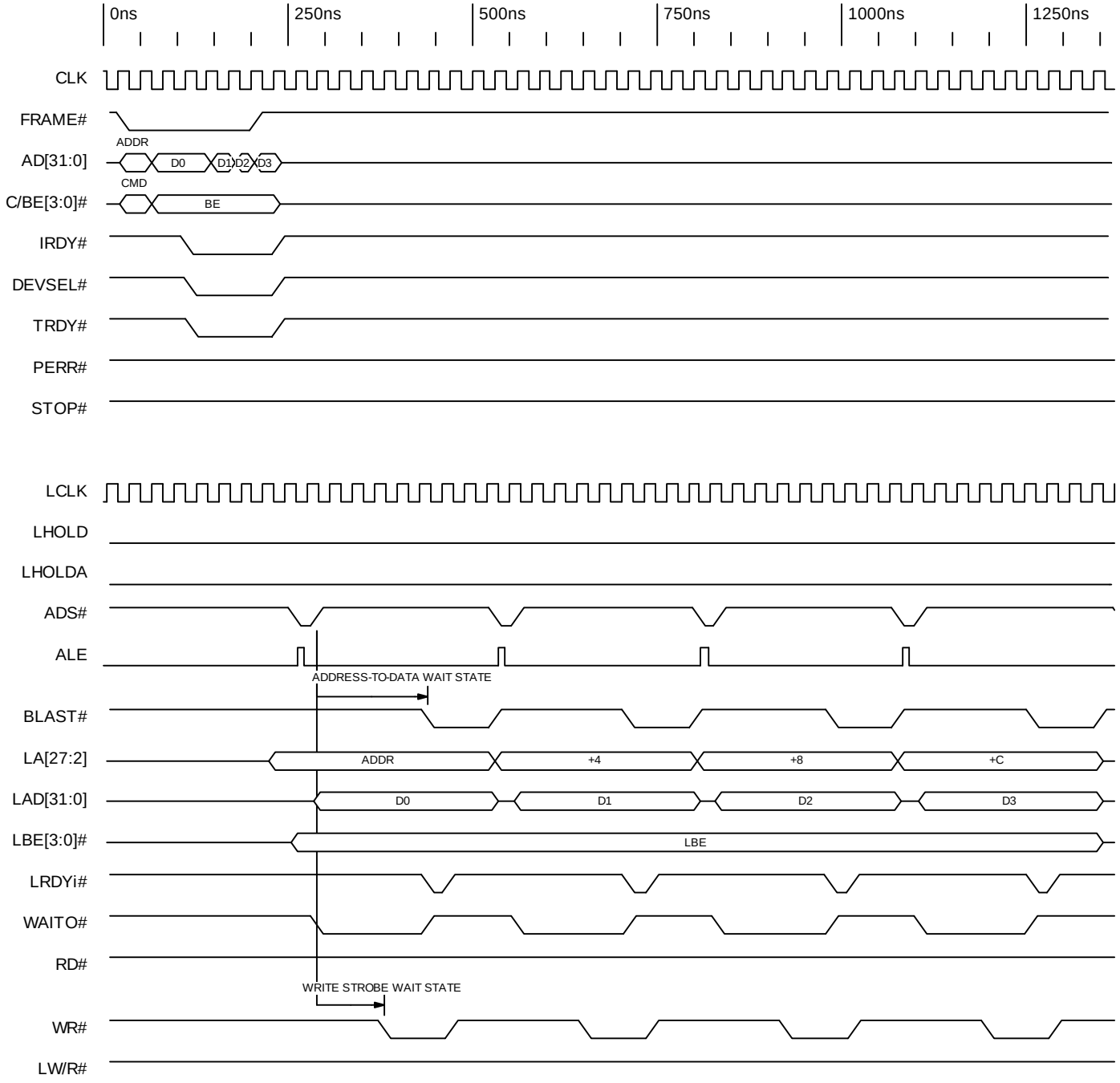
Timing Diagram 9-9. Direct Slave Single Read without Wait States (32-Bit Local Bus)



Single read, 32-bit local bus, with wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe = zero wait states

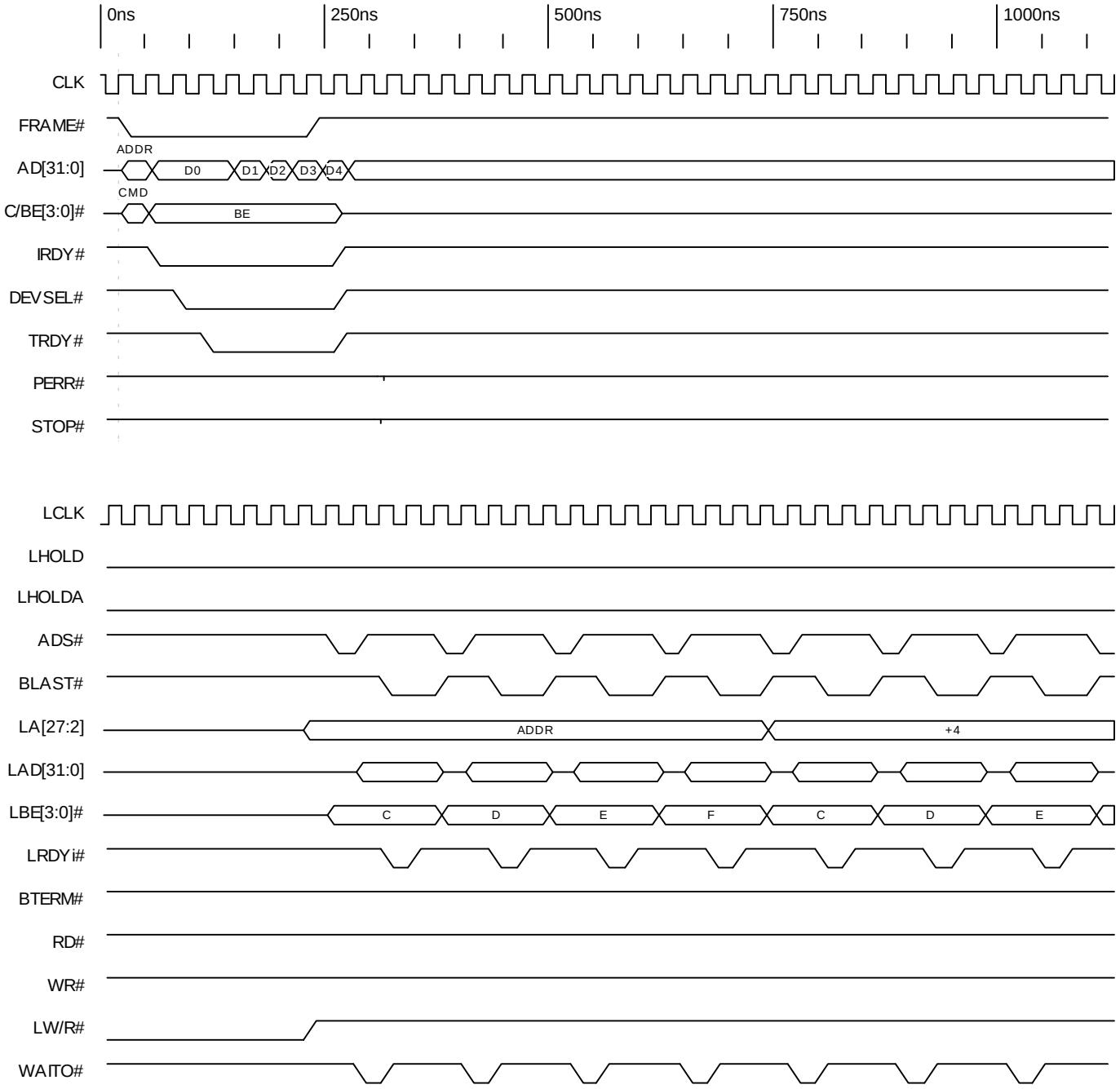
Timing Diagram 9-10. Direct Slave Single Read with Wait States (32-Bit Local Bus)

9.1.3 Direct Slave Non-Burst



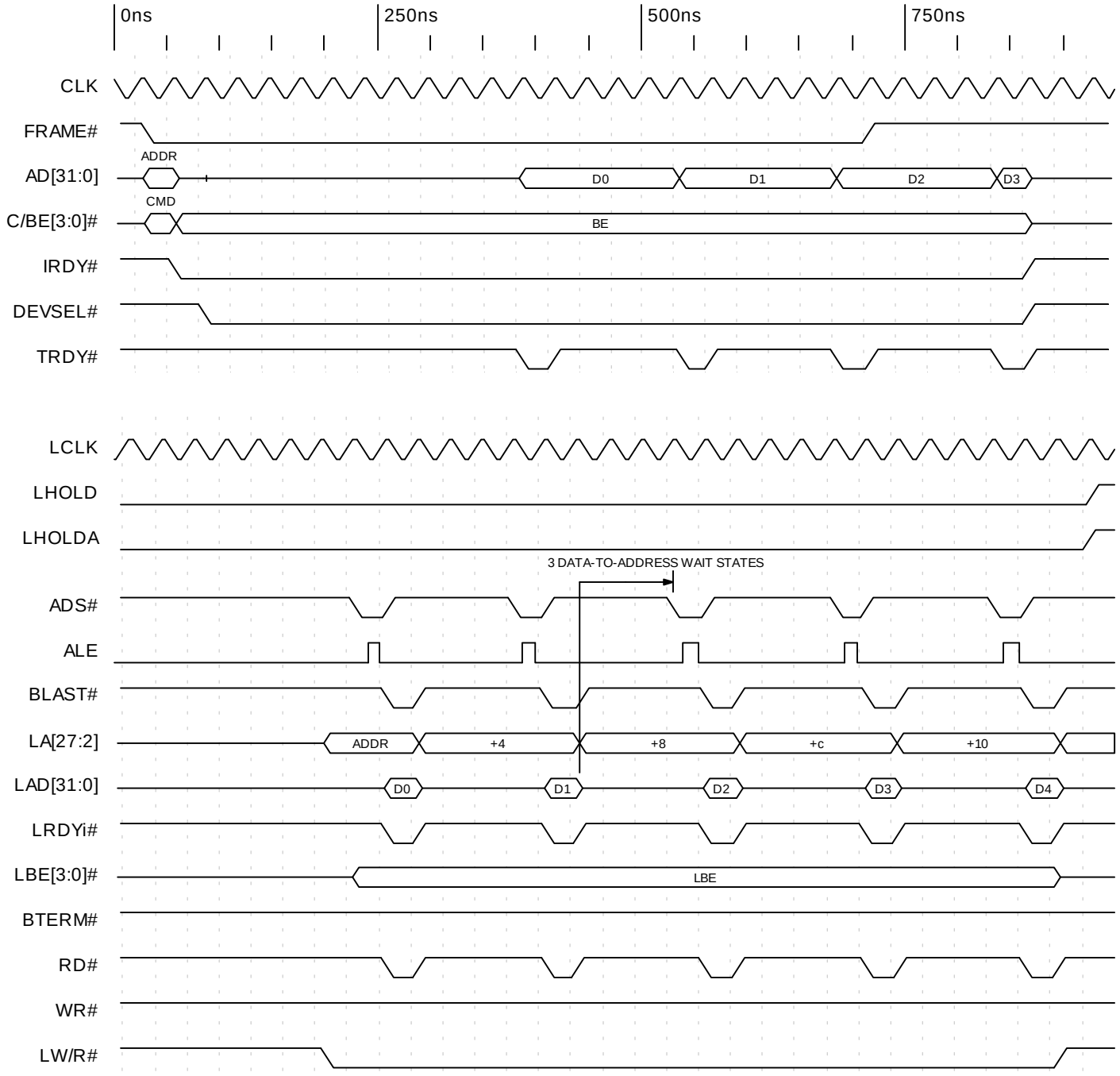
Non-burst write of four Lwords
32-bit local bus, BTERM# is disabled
Address-to-data = five wait states
Data-to-data = one wait state
Write strobe = three wait states
Write cycle hold = two wait states

Timing Diagram 9-11. Direct Slave Non-Burst Write with Wait States (32-Bit Local Bus)



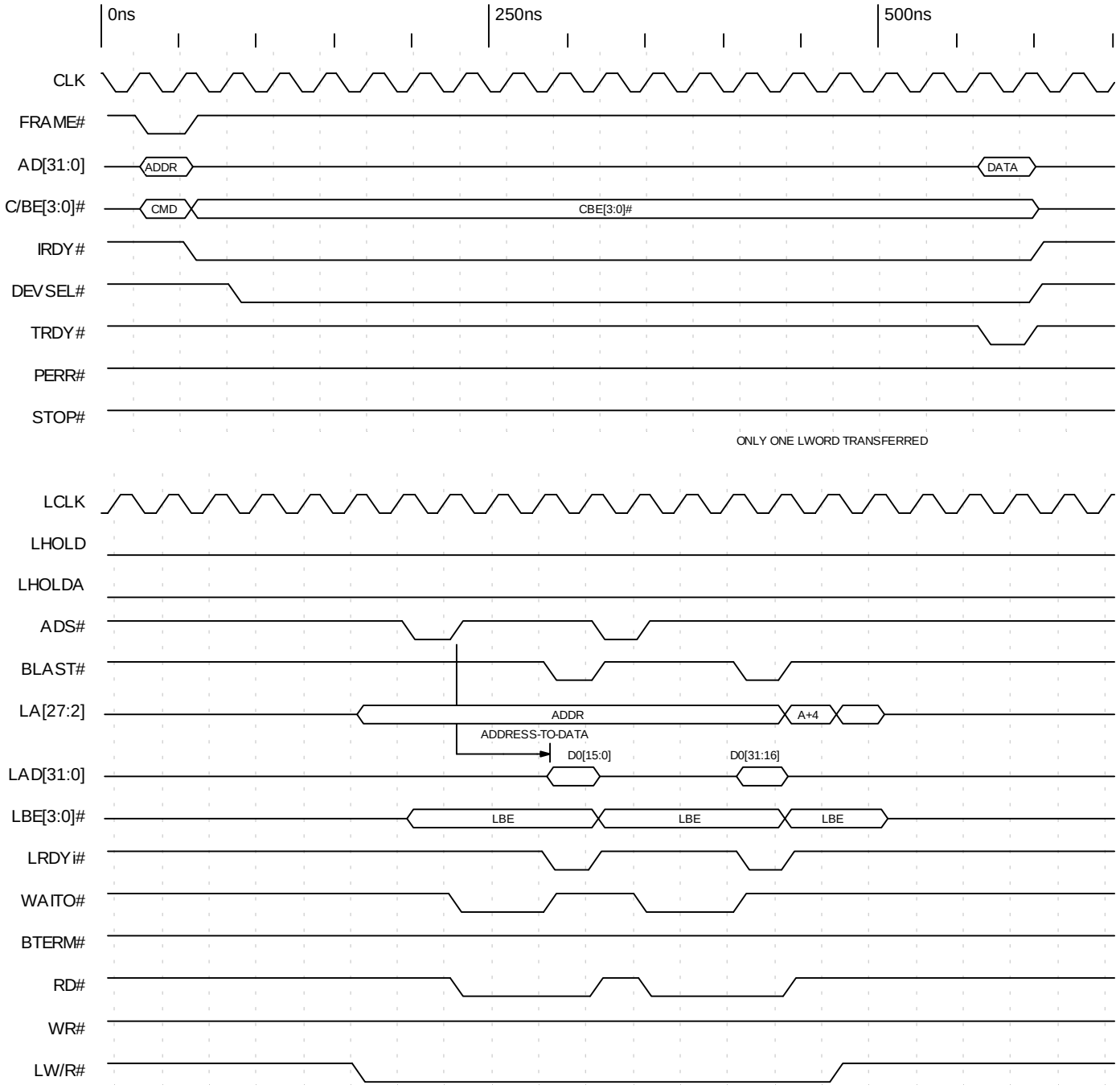
Non-burst write of five Lwords
8-bit local bus
Address-to-data = one wait state
Data-to-data = zero wait states
Two wait states = WR# non-asserted
Write hold cycle = one wait state

Timing Diagram 9-12. Direct Slave Non-Burst Write (8-Bit Local Bus)



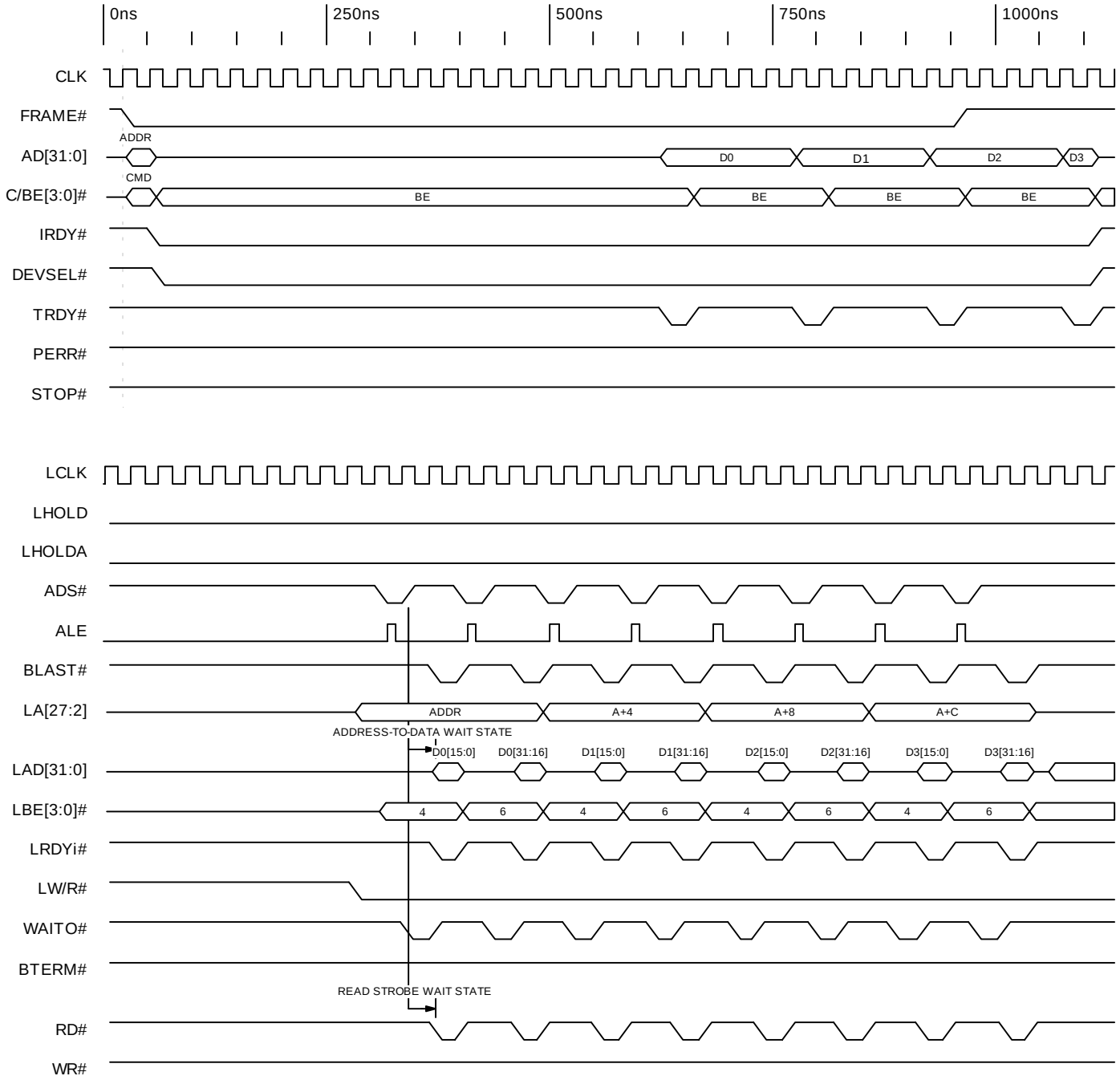
Direct slave read from Space 1
Burst disabled, BTERM# enabled
Local bus: Little Endian, 32 bit
Data-to-address = three wait states
Write strobe = zero wait states
Write cycle hold = zero wait states

Timing Diagram 9-13. Direct Slave Non-Burst Read with BTERM# Enabled (32-Bit Local Bus)



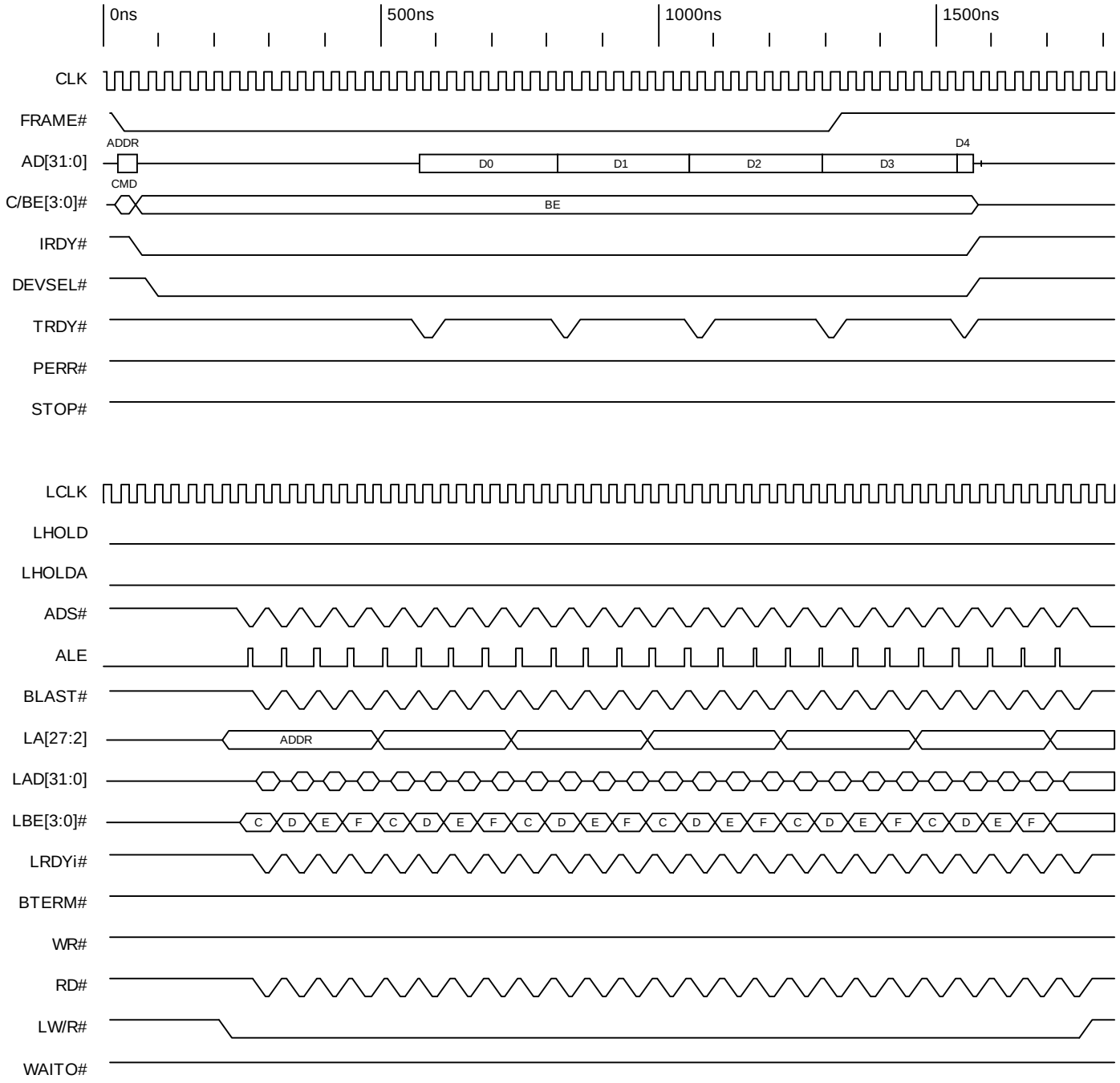
16-bit local bus
Address-to-data = two wait states
Data-to-data = zero wait states
Read strobe = zero wait states

Timing Diagram 9-14. Direct Slave Non-Burst Read with Unaligned PCI Address (32-Bit Local Bus)



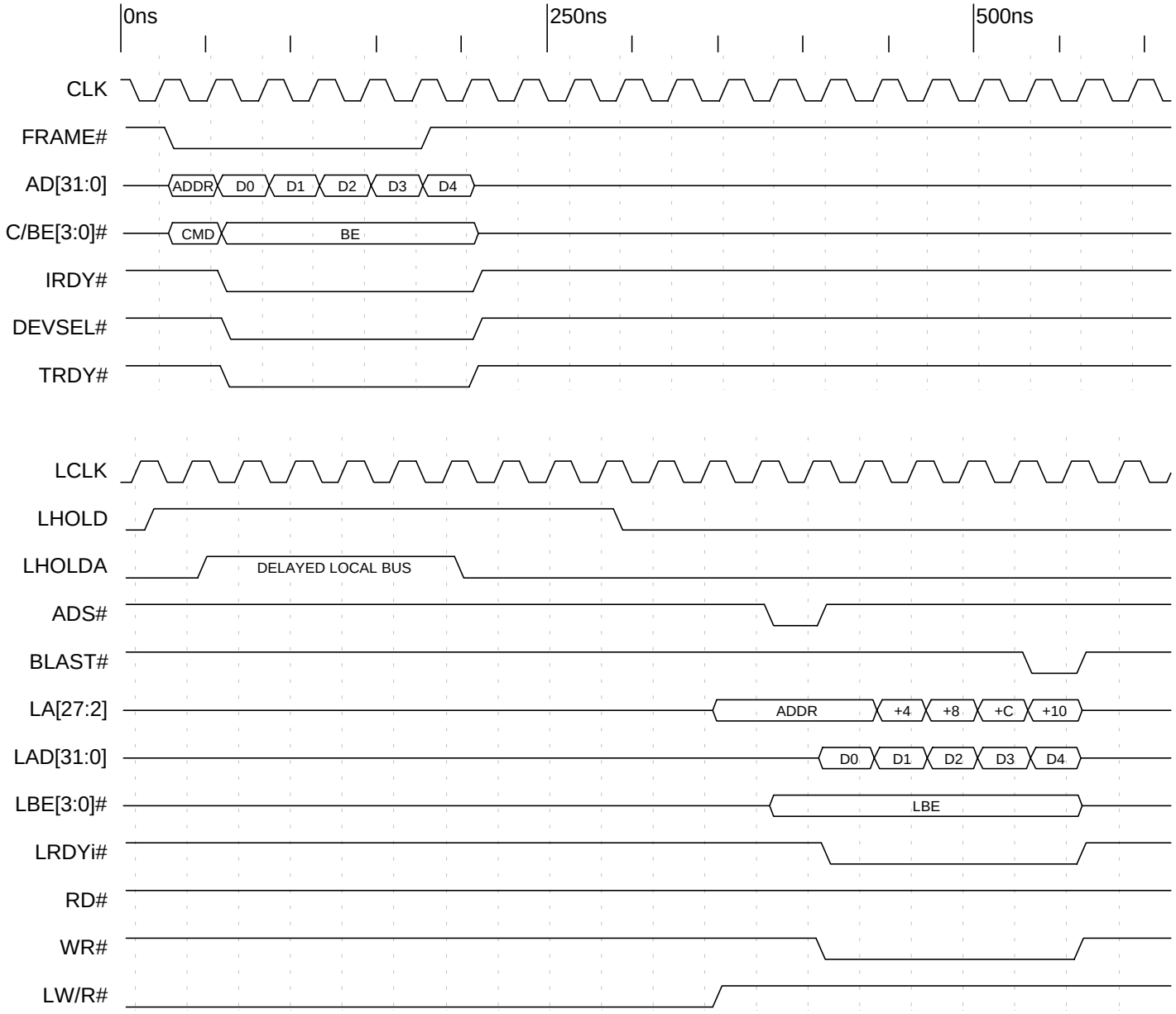
Address-to-data = one wait state
Non-burst read of four Lwords
Prefetch four Lwords
16-bit local bus
Data-to-data = one wait state
Read strobe = one wait state

Timing Diagram 9-15. Direct Slave Non-Burst Read with Prefetch (16-Bit Local Bus)

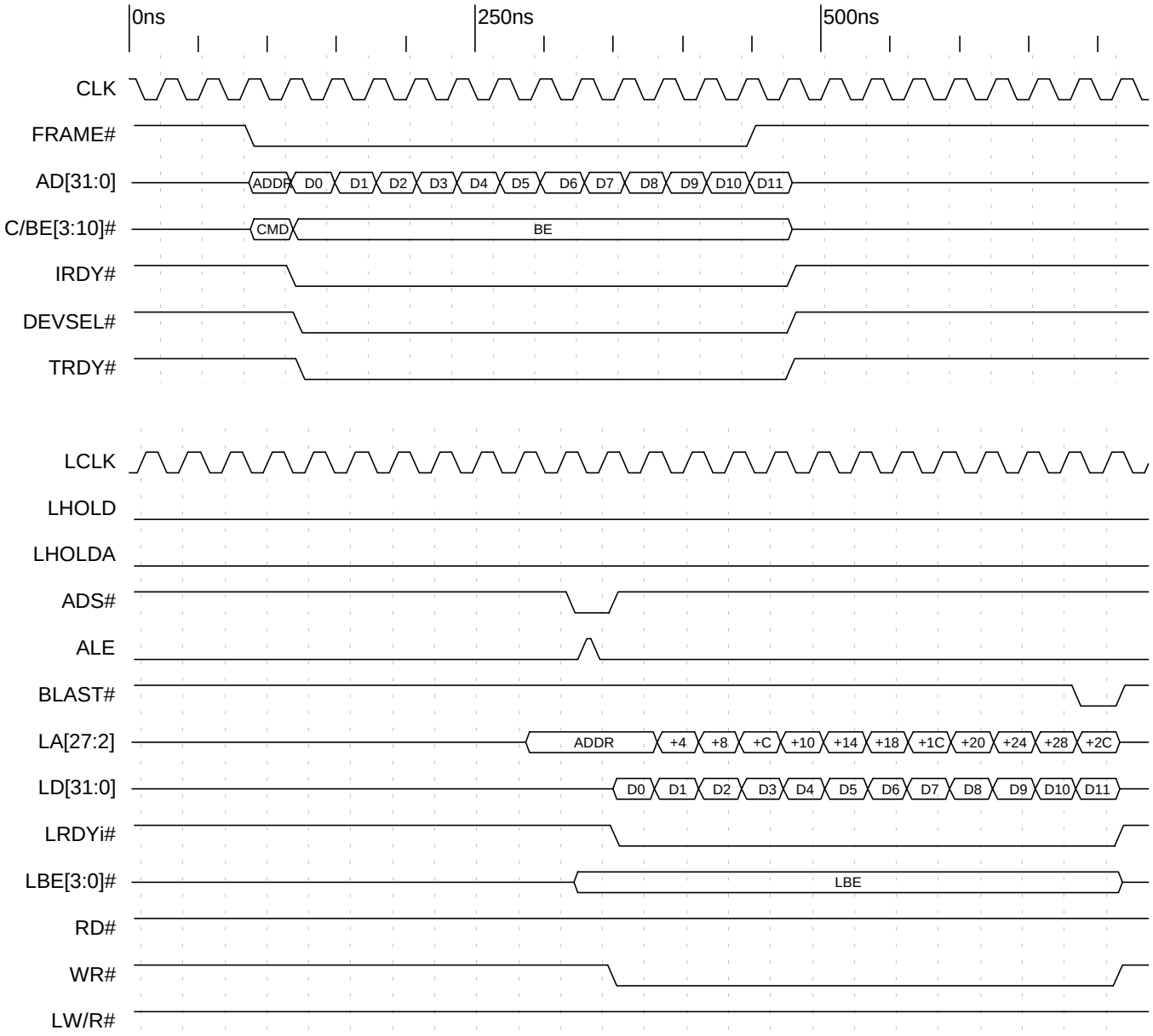


Timing Diagram 9-16. Direct Slave Non-Burst Read with Prefetch (8-Bit Local Bus)

9.1.4 Direct Slave Burst

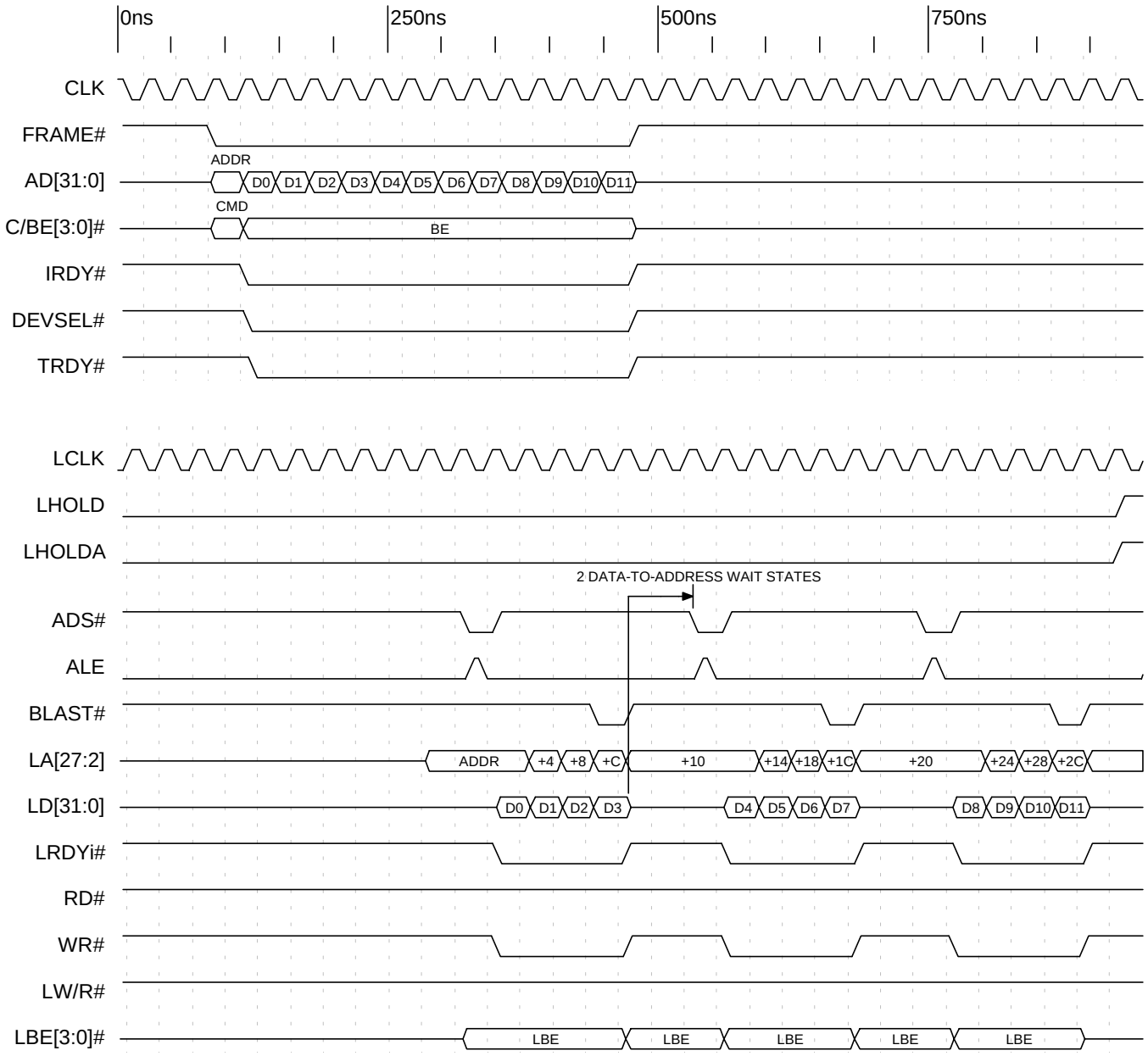


Timing Diagram 9-17. Direct Slave Burst Write with Delayed Local Bus (32-Bit Local Bus)



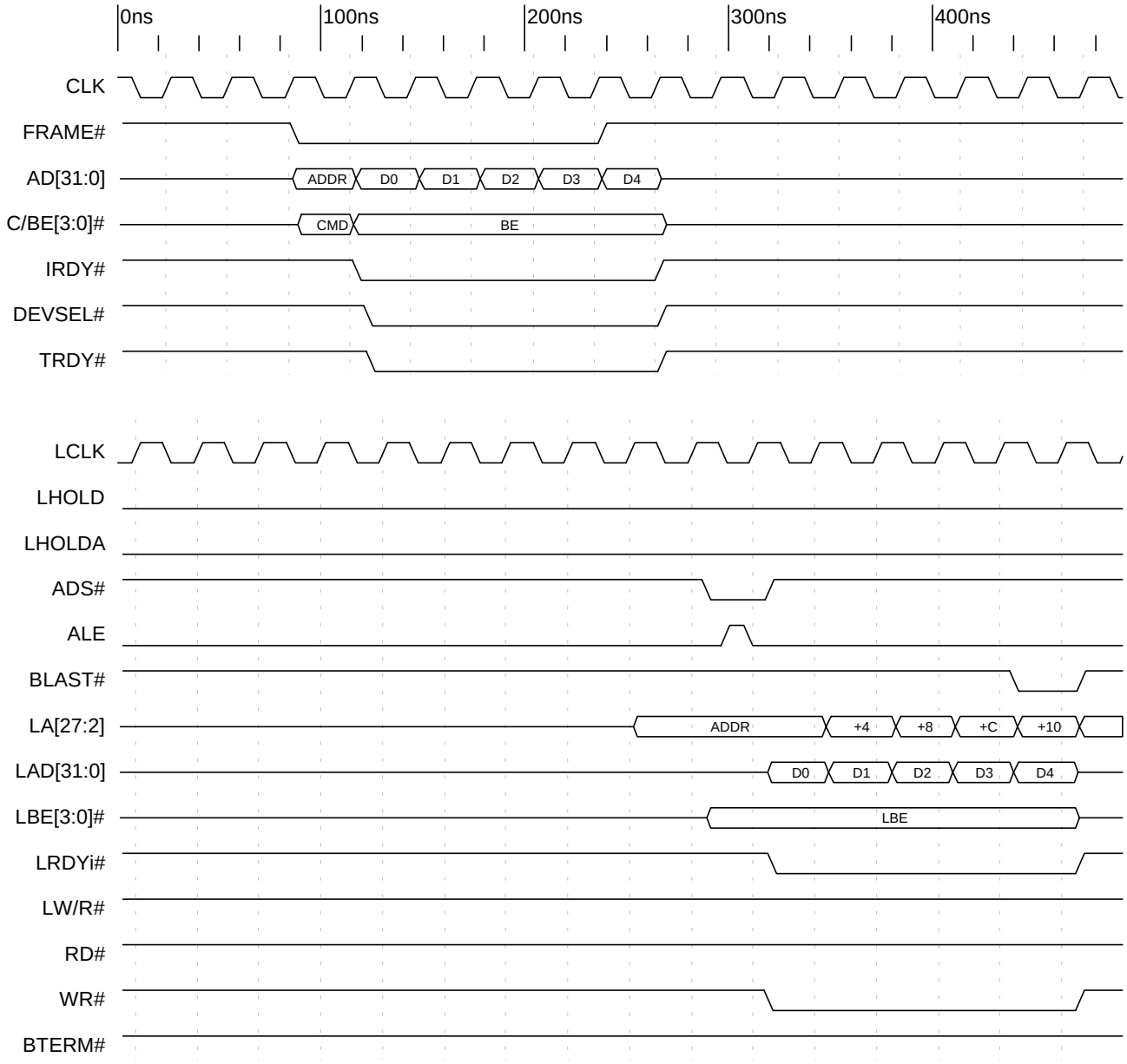
For Space 2 (same for Space 0, 1, and 3, and expansion ROM)
Local bus: Little Endian, 32 bit
Burst enabled (burst write of 12 Lwords), BTERM# enabled

Timing Diagram 9-18. Direct Slave Burst Write with BTERM# Enabled (32-Bit Local Bus)



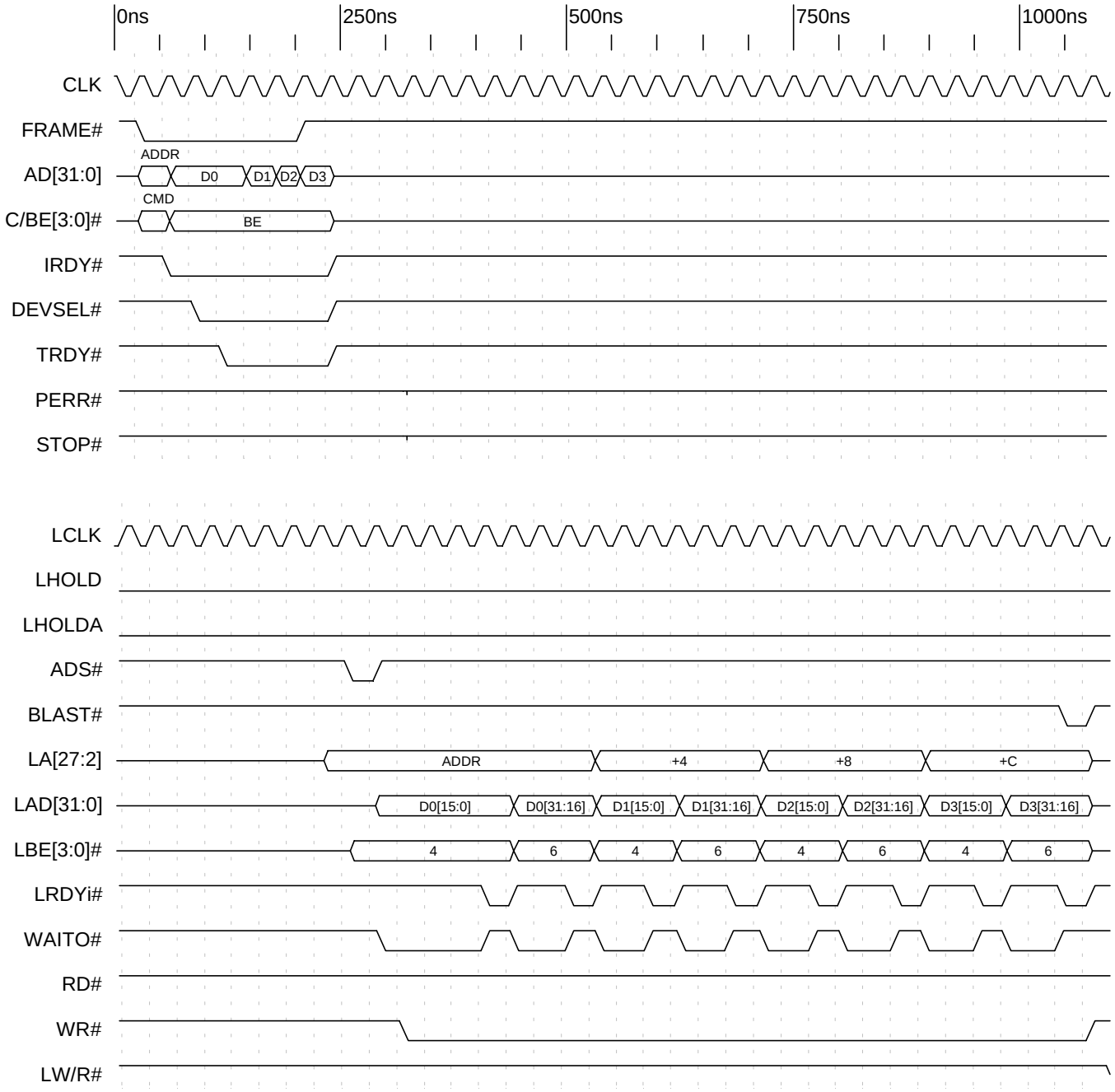
For Space 2 (same for Space 0, 1, and 3, and expansion ROM)
Local bus: Little Endian, 32 bit
Burst enabled (burst write of four Lwords), BTERM# disabled
Data-to-address = two wait states

Timing Diagram 9-19. Direct Slave Burst Write with BTERM# Disabled and Wait States (32-Bit Local Bus)



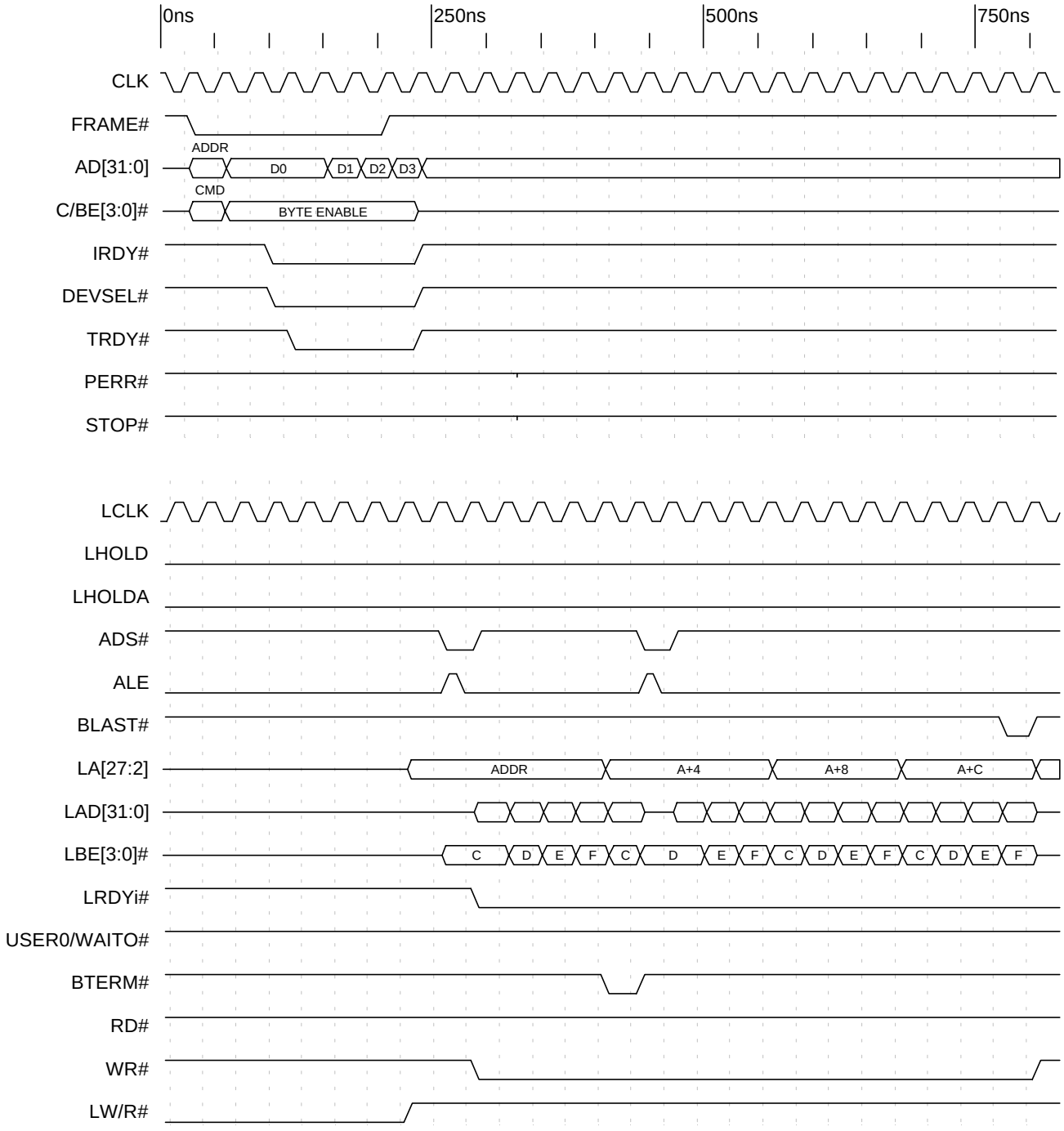
Local bus: Little Endian, 32 bit
Burst enabled (burst write of five Lwords), BTERM# enabled
Address-to-data = zero wait states
Data-to-data = zero wait states
Write strobe = zero wait states
Write cycle hold = zero wait states

Timing Diagram 9-20. Direct Slave Burst Write with BTERM# Enabled (32-Bit Local Bus)



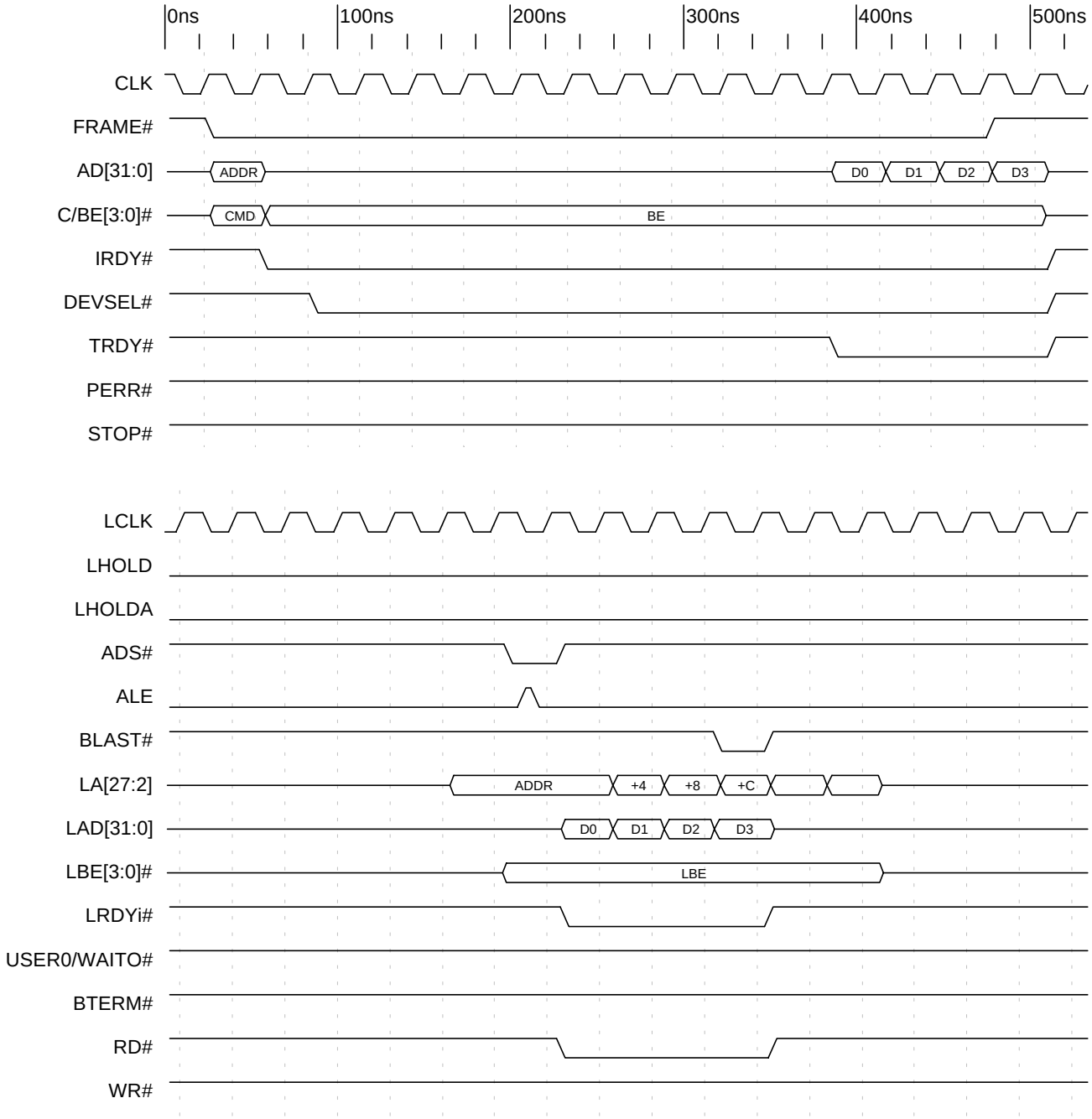
Burst enabled (burst write of four Lwords)
Address-to-data = four wait states
Data-to-data = two wait states
Write strobe = one wait state
Write cycle hold = zero wait states

Timing Diagram 9-21. Direct Slave Burst Write (16-Bit Local Bus)



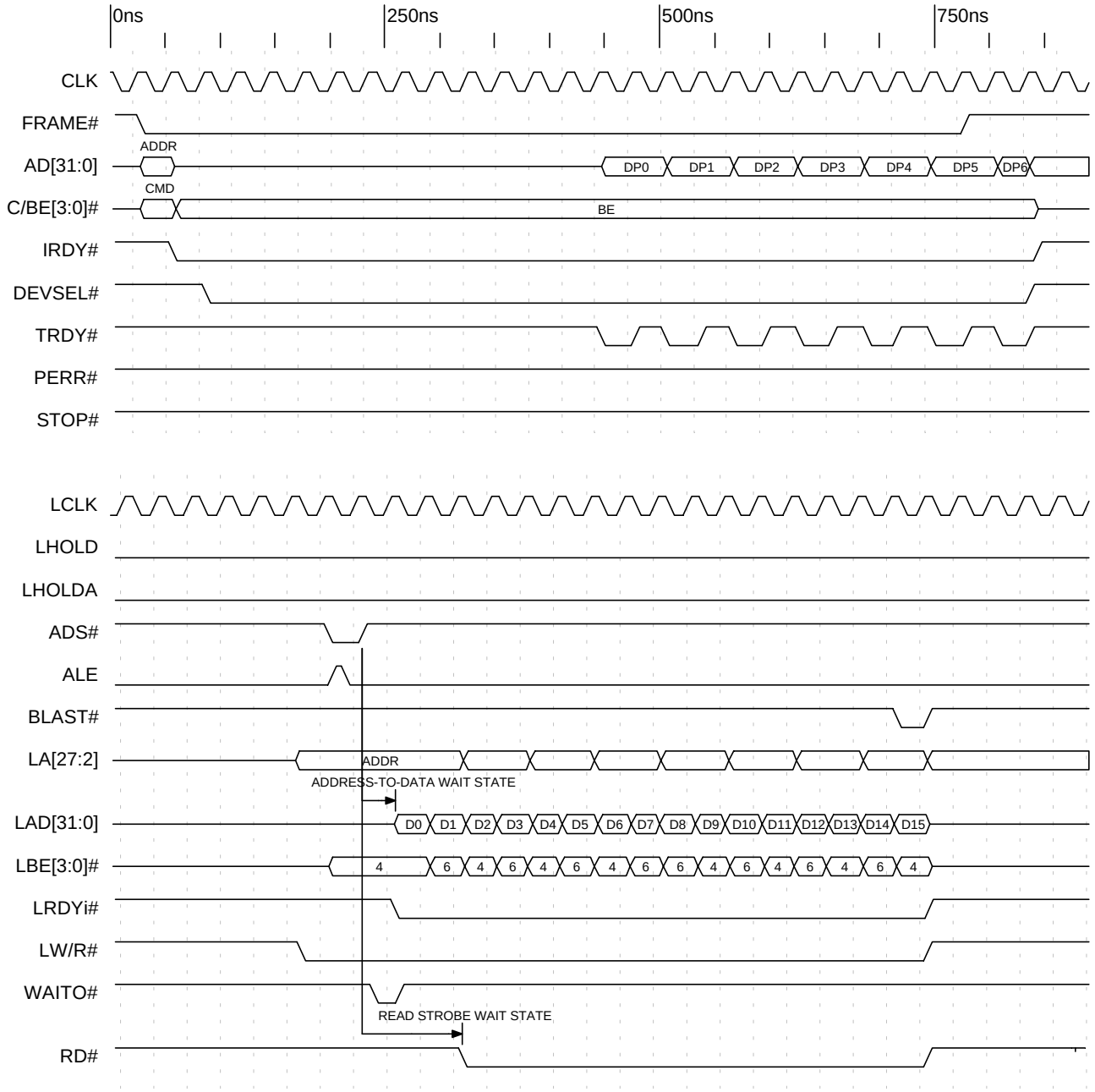
Burst enabled (burst write of four Lwords), BTERM# enabled

Timing Diagram 9-22. Direct Slave Burst Write with BTERM# Enabled (8-Bit Local Bus)



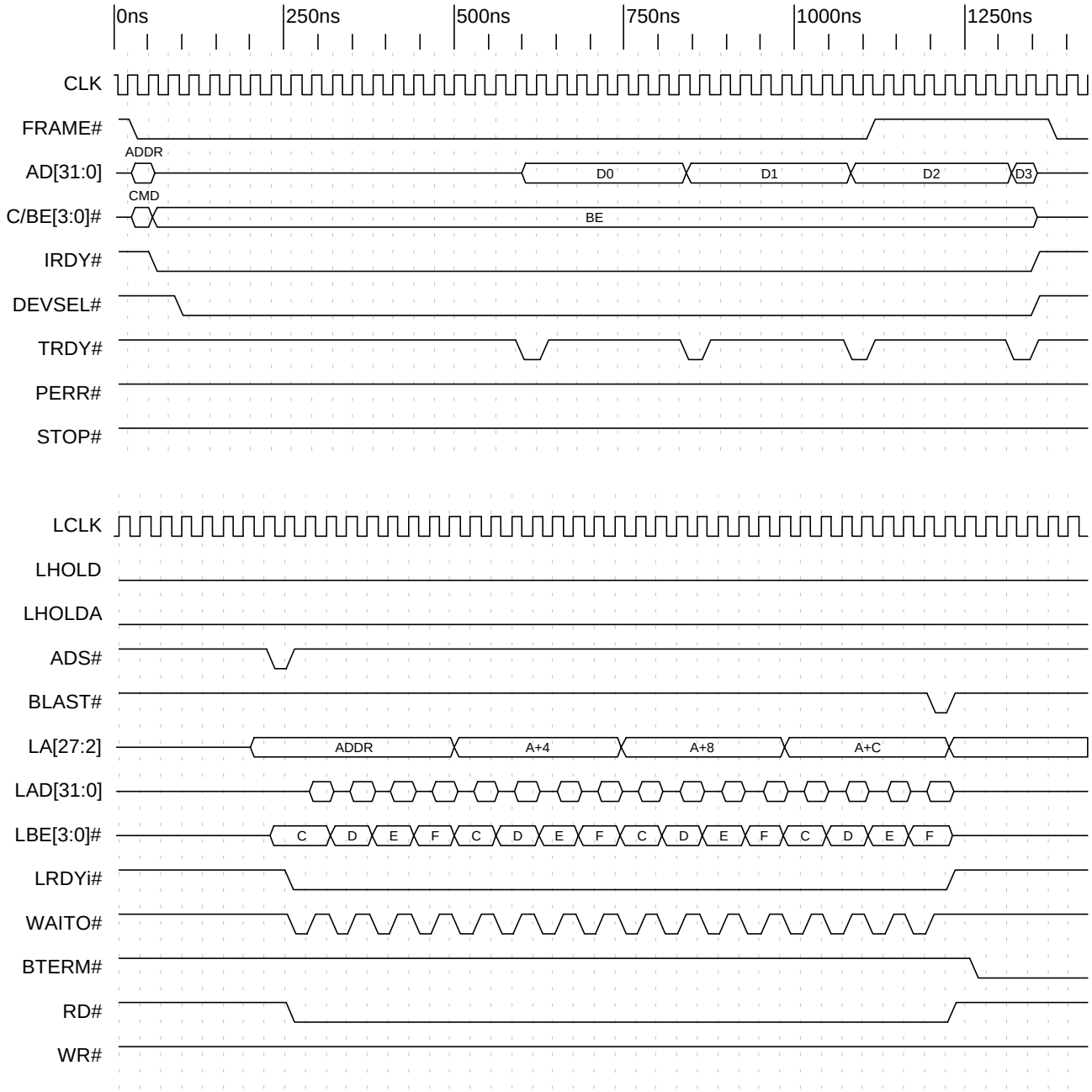
Local burst
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe = zero wait states

Timing Diagram 9-23. Direct Slave Burst Read with Prefetch of Four Lwords (32-Bit Local Bus)



Burst read eight Lwords
Address-to-data = one wait state
Data-to-data = zero wait states
Read strobe = three wait states

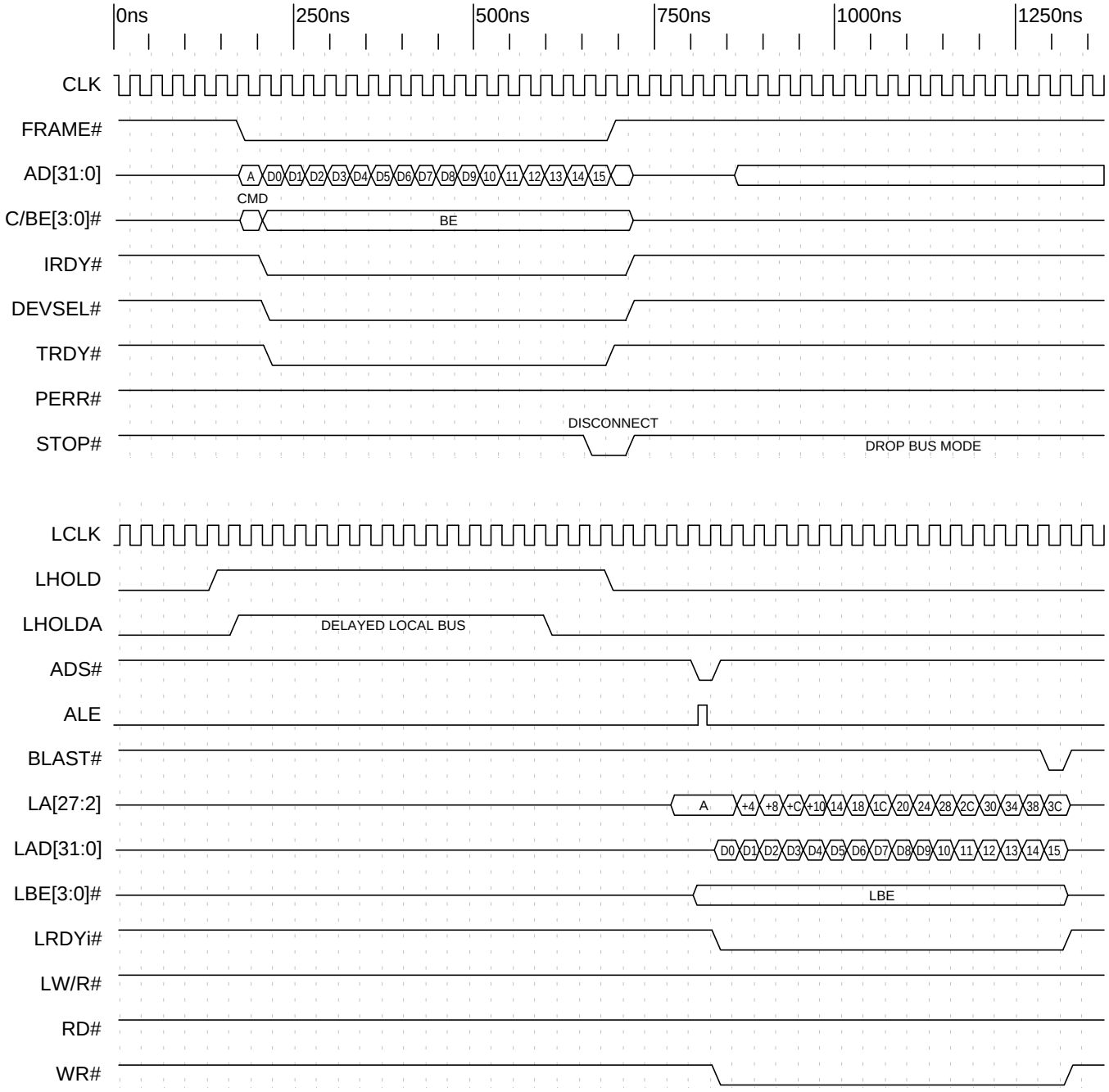
Timing Diagram 9-24. Direct Slave Burst Read with Prefetch of Eight Lwords (16-Bit Local Bus)



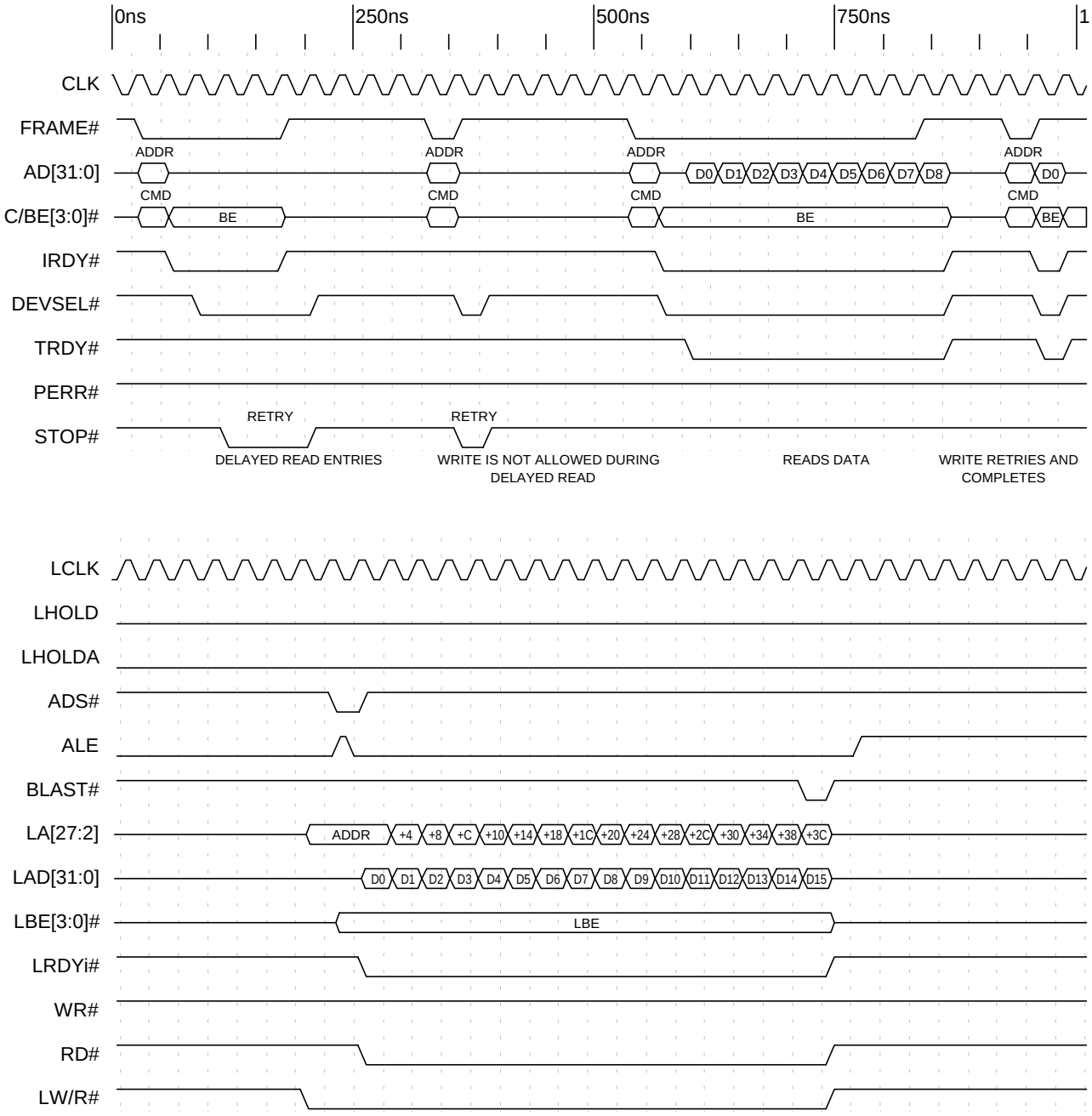
Direct slave, Burst read four Lwords
8-bit local bus
Address-to-data = one wait state
Data-to-data = one wait state
Read strobe = zero wait states

Timing Diagram 9-25. Direct Slave Burst Read with Prefetch of Four Lwords (8-Bit Local Bus)

9.1.5 Miscellaneous Functionality

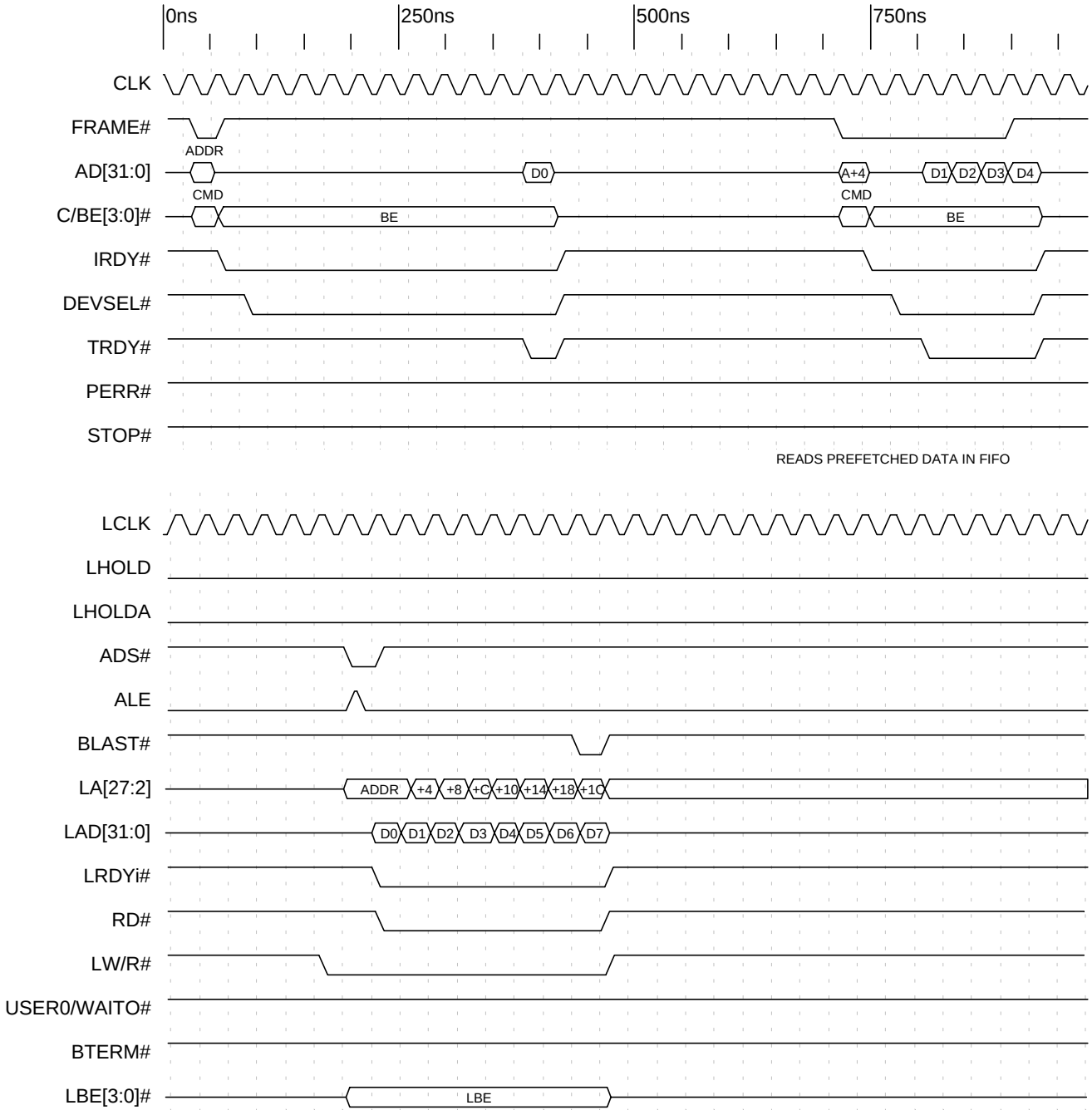


Timing Diagram 9-26. Direct Slave Write PCI Spec v2.1



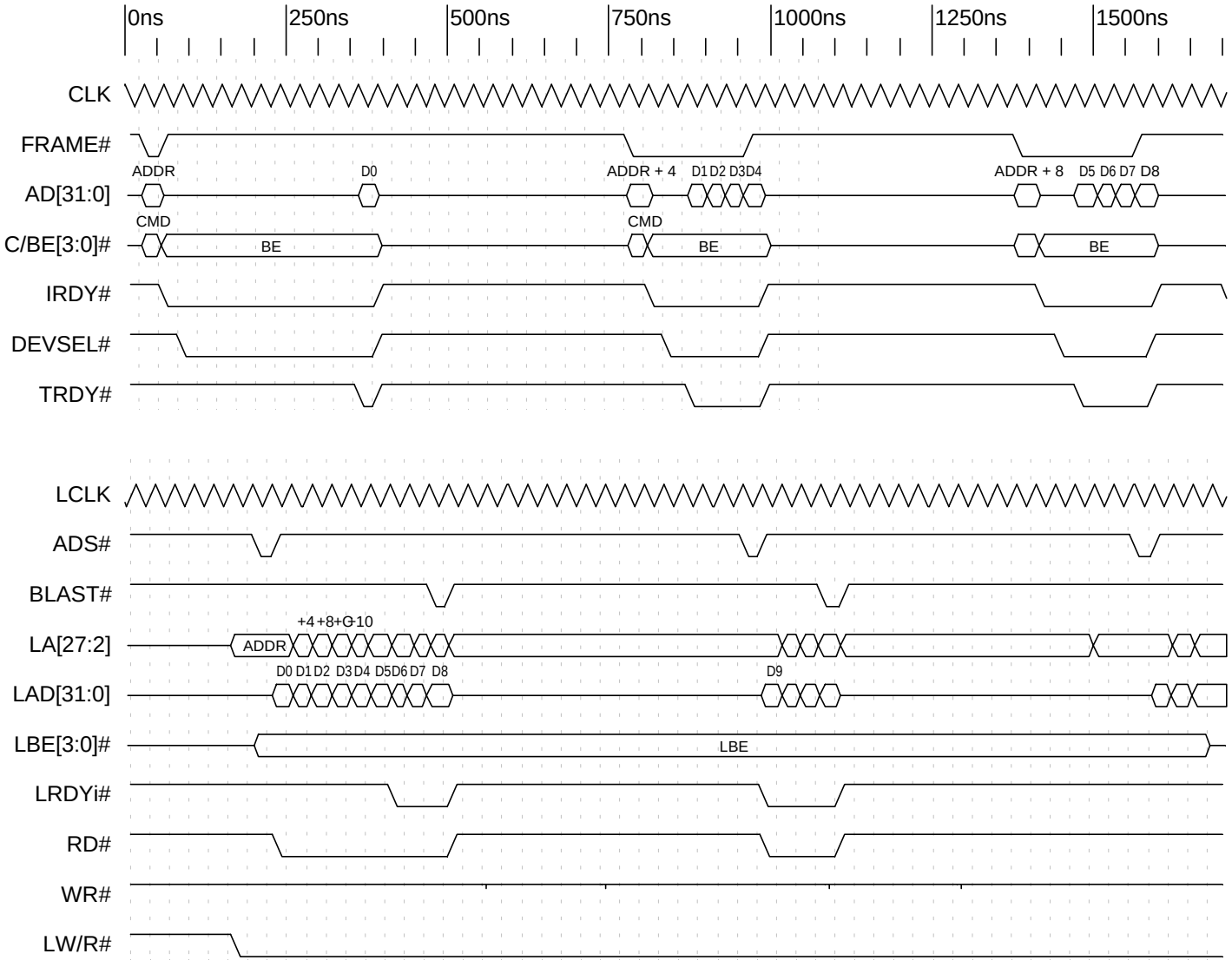
Disconnect immediately for a read
Does not effect pending reads when write cycle occurs
Does not flush the read FIFO if PCI ready cycle completes
Force Retry on write if read is pending
De-assert TRDY# until space is available in the direct slave write FIFO

Timing Diagram 9-27. Direct Slave Read PCI Spec v2.1

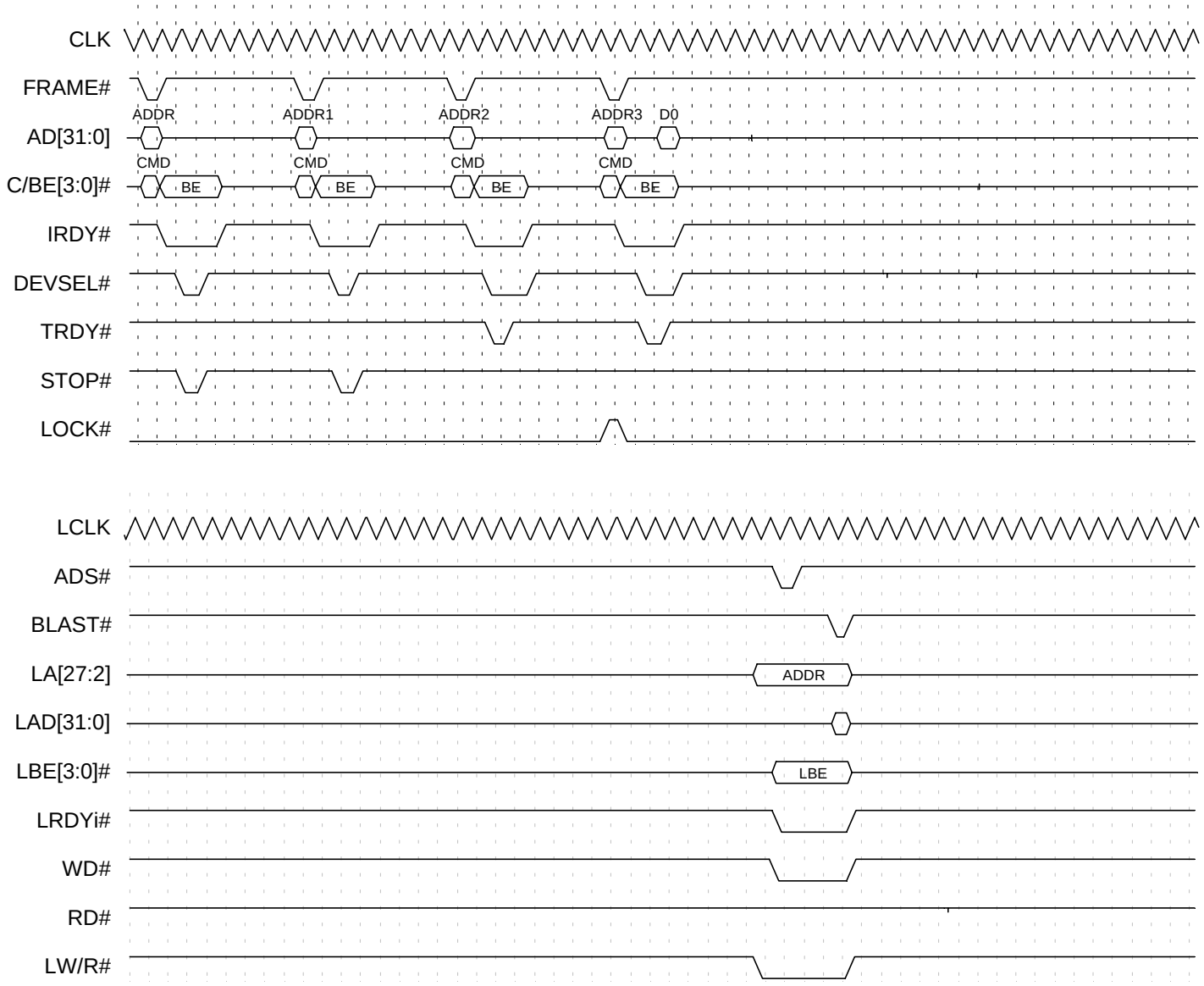


Direct slave read for Space 0 (same for Space 1, 2, and 3, and expansion ROM)
Prefetch eight Lwords, 32-bit local bus

Timing Diagram 9-28. Direct Slave Read with Read Ahead Mode Enabled

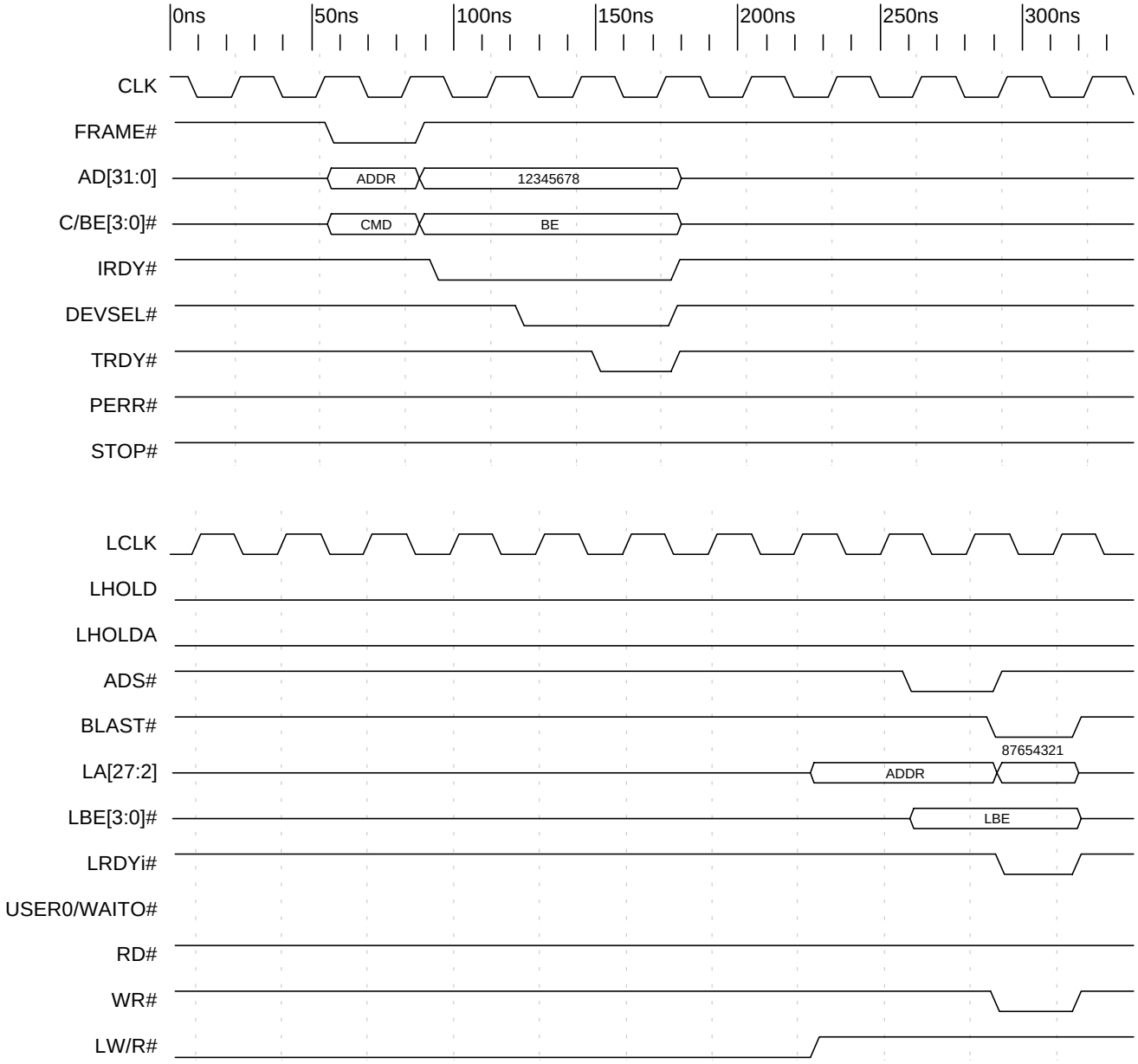


Timing Diagram 9-29. Read Ahead Mode

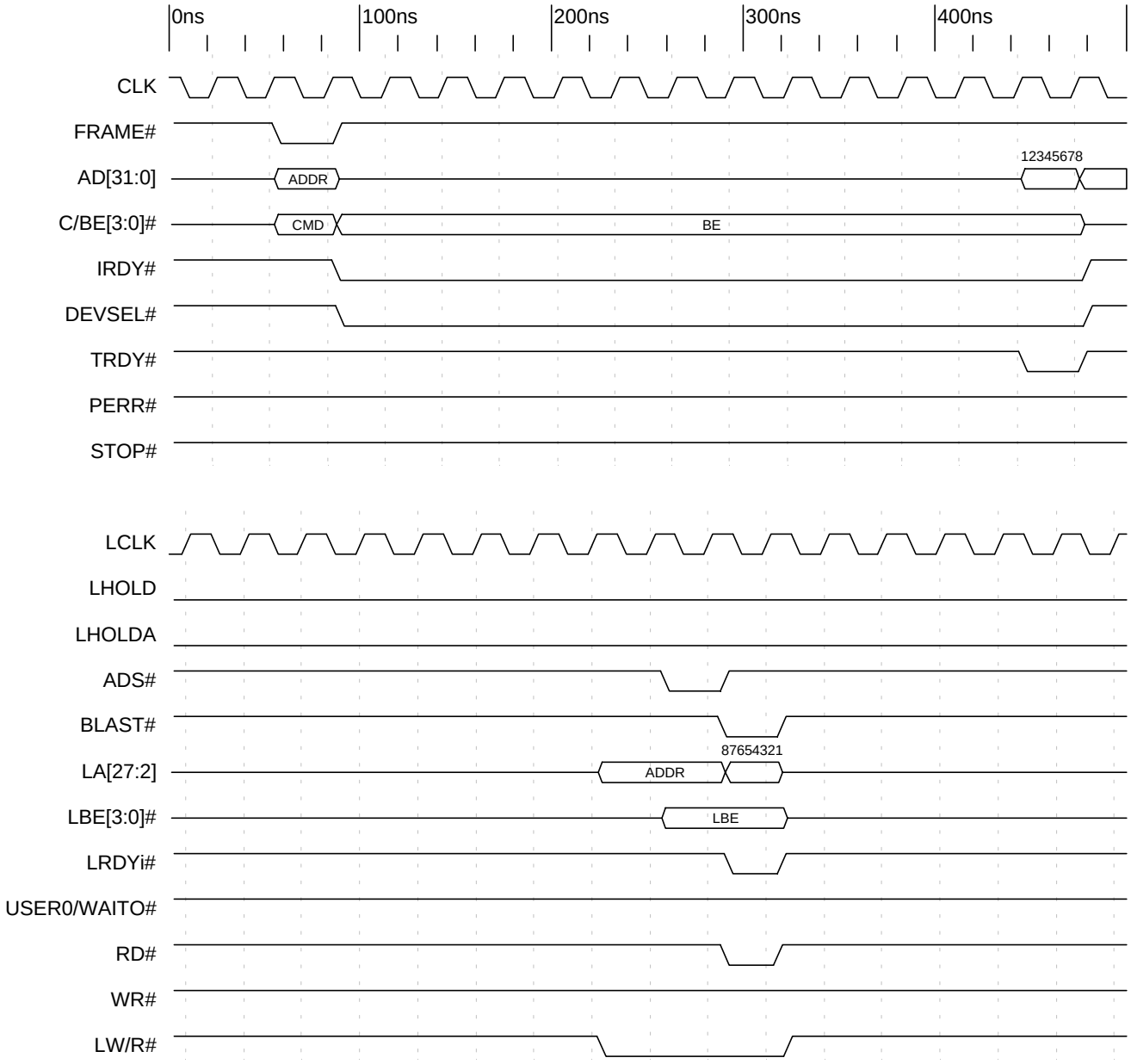


Timing Diagram 9-30. PCI Lock Mode

9.1.6 Big Endian Mode and Multiplexed Local Bus (J Mode)

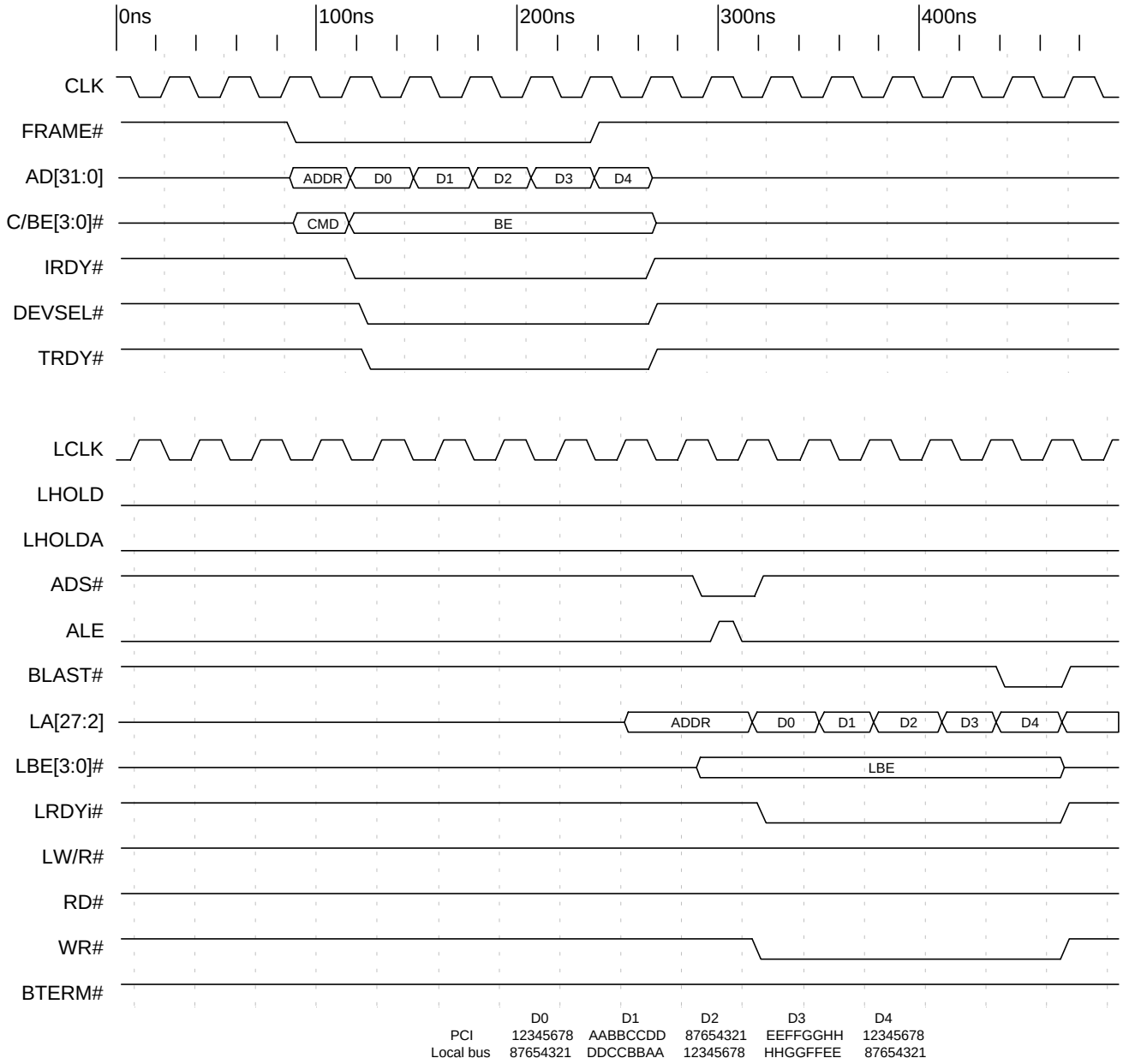


Timing Diagram 9-31. Direct Slave Single Write to 32-Bit Local Bus Big Endian and Multiplexed Local Bus (J Mode)



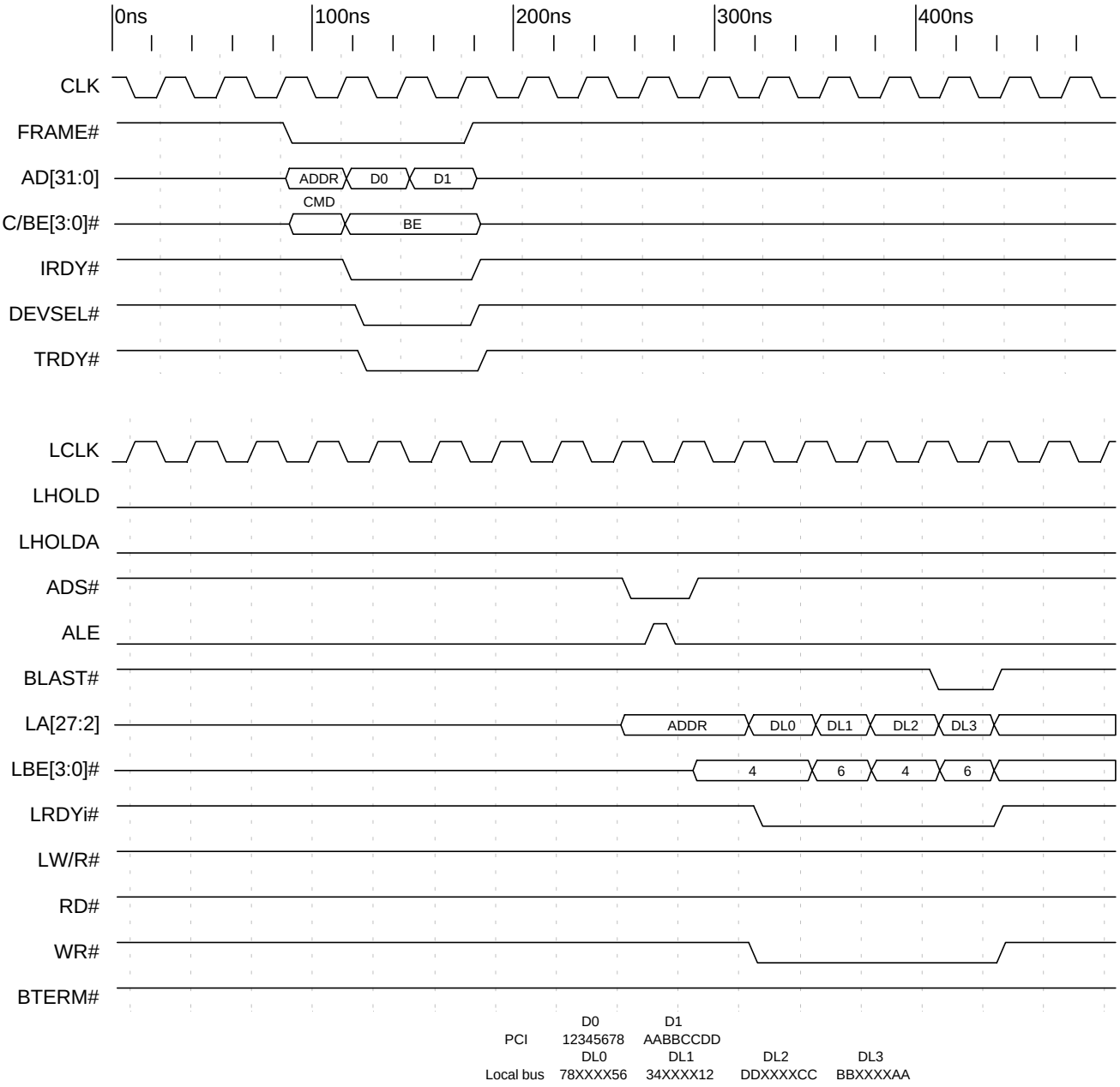
Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe = zero wait states

Timing Diagram 9-32. Direct Slave Single Read from 32-Bit Local Bus Big Endian and Multiplexed Local Bus (J Mode)



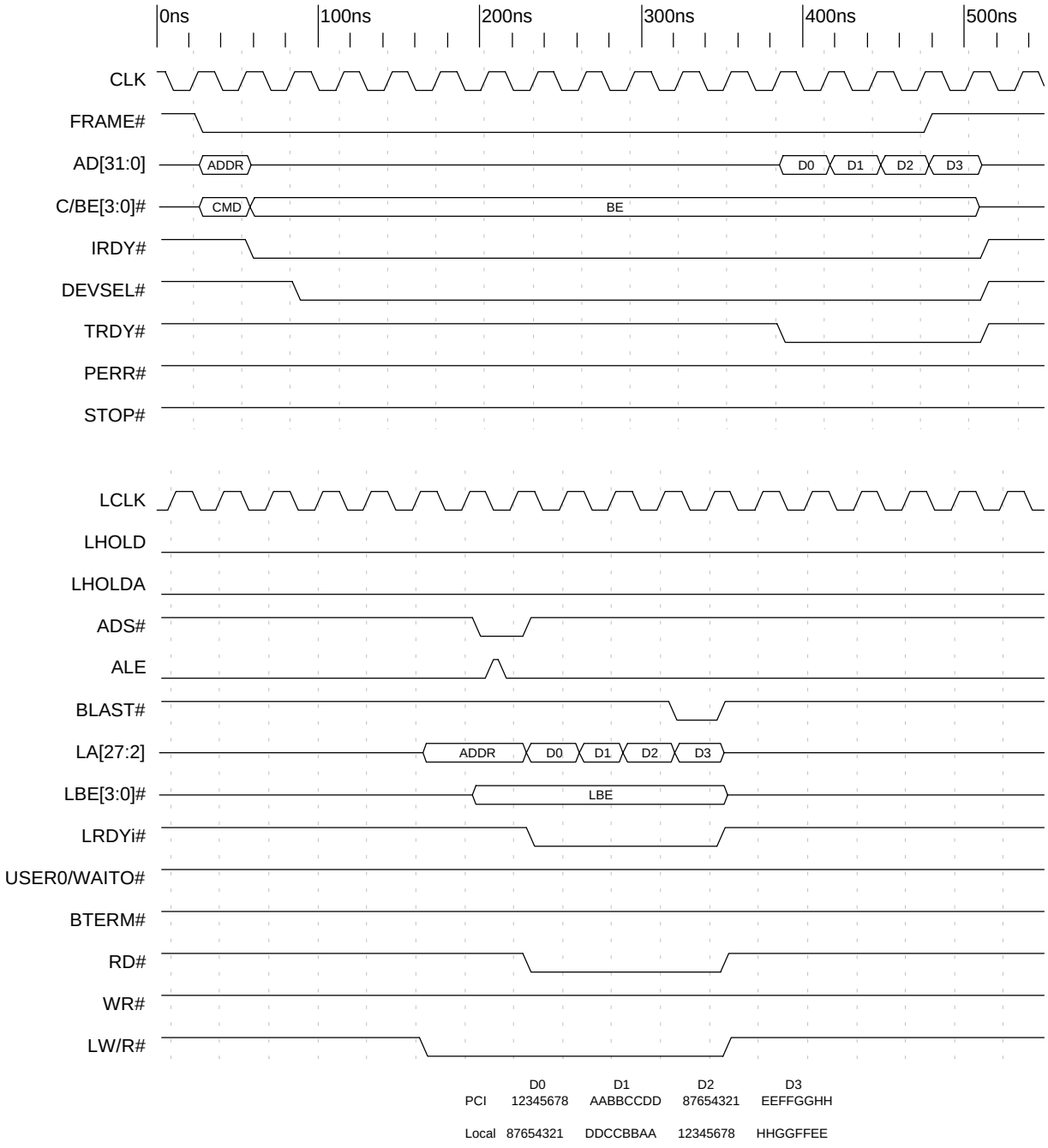
Burst enabled (burst write of five Lwords), BTERM# enabled
Local bus: Big Endian, 32 bit
Address-to-data = zero wait states
Write strobe = zero wait states
Write cycle hold = zero wait states

Timing Diagram 9-33. Direct Slave Burst Write and Multiplexed Local Bus (32-Bit Local Bus, J Mode)



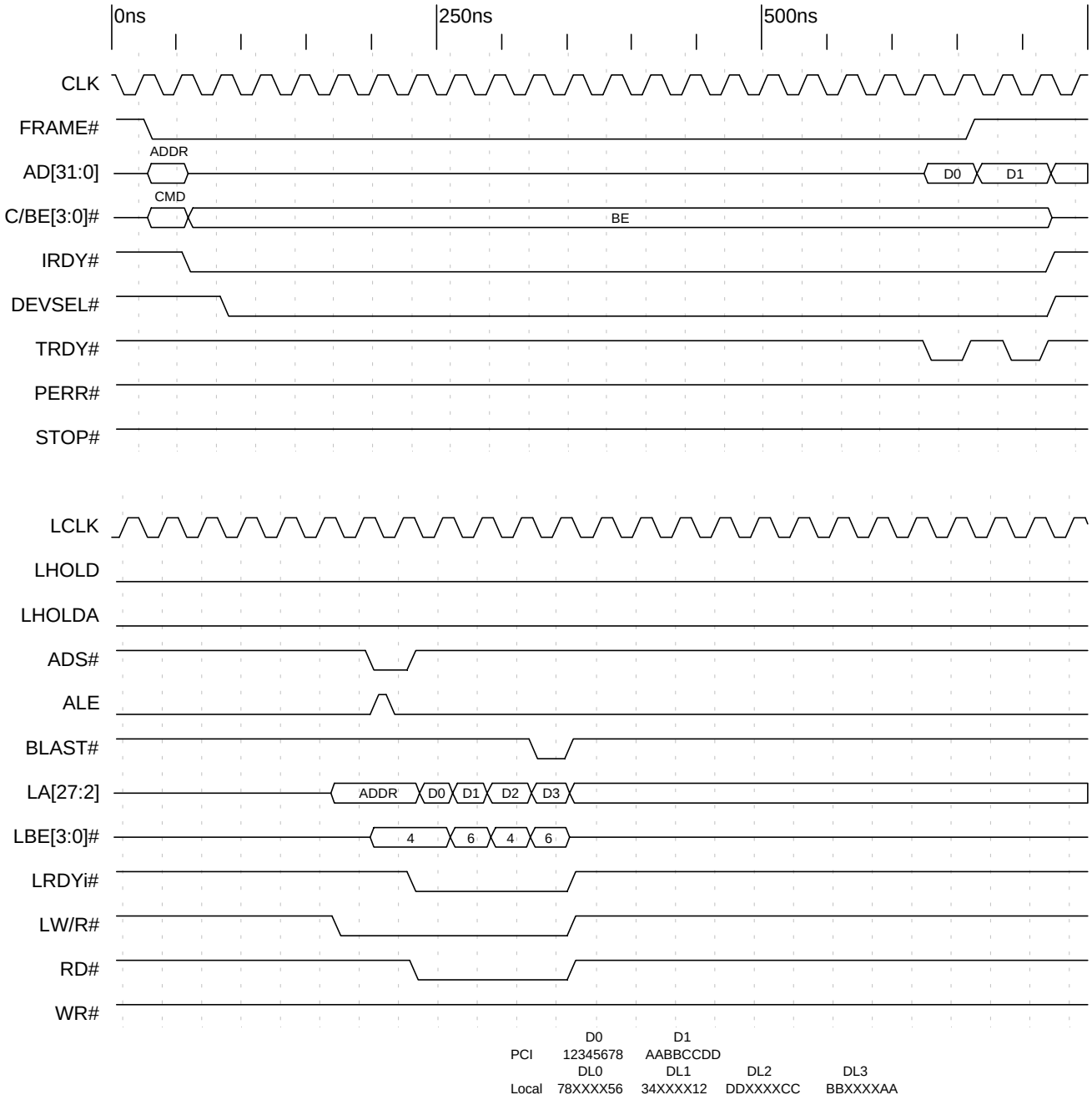
Burst enabled (burst write of four Lwords), BTERM# enabled
Local bus: Big Endian, 16 bit
Address-to-data = zero wait states
Write strobe = zero wait states
Write cycle hold = zero wait states

Timing Diagram 9-34. Direct Slave Burst Write and Multiplexed Local Bus (16-Bit Local Bus, J Mode)



Prefetch four Lwords, Local burst
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe = zero wait states

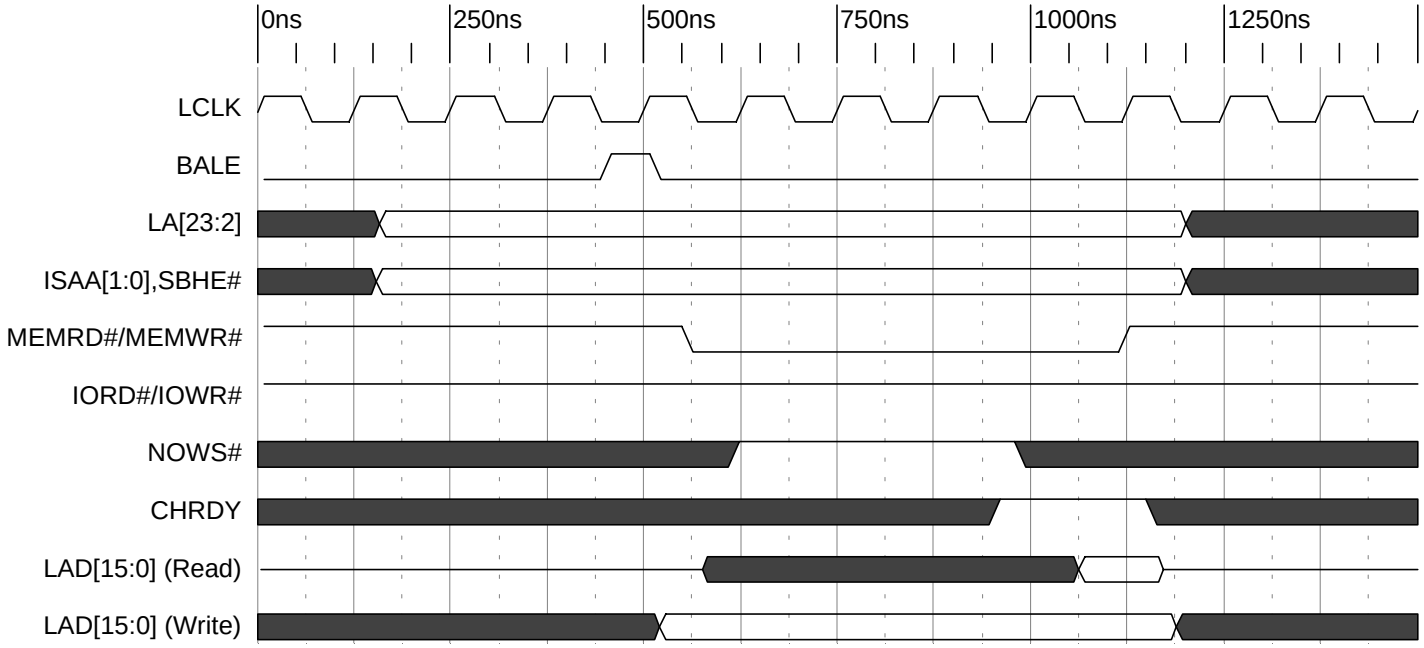
Timing Diagram 9-35. Direct Slave Burst Read and Multiplexed Local Bus (32-Bit Local Bus, J Mode)



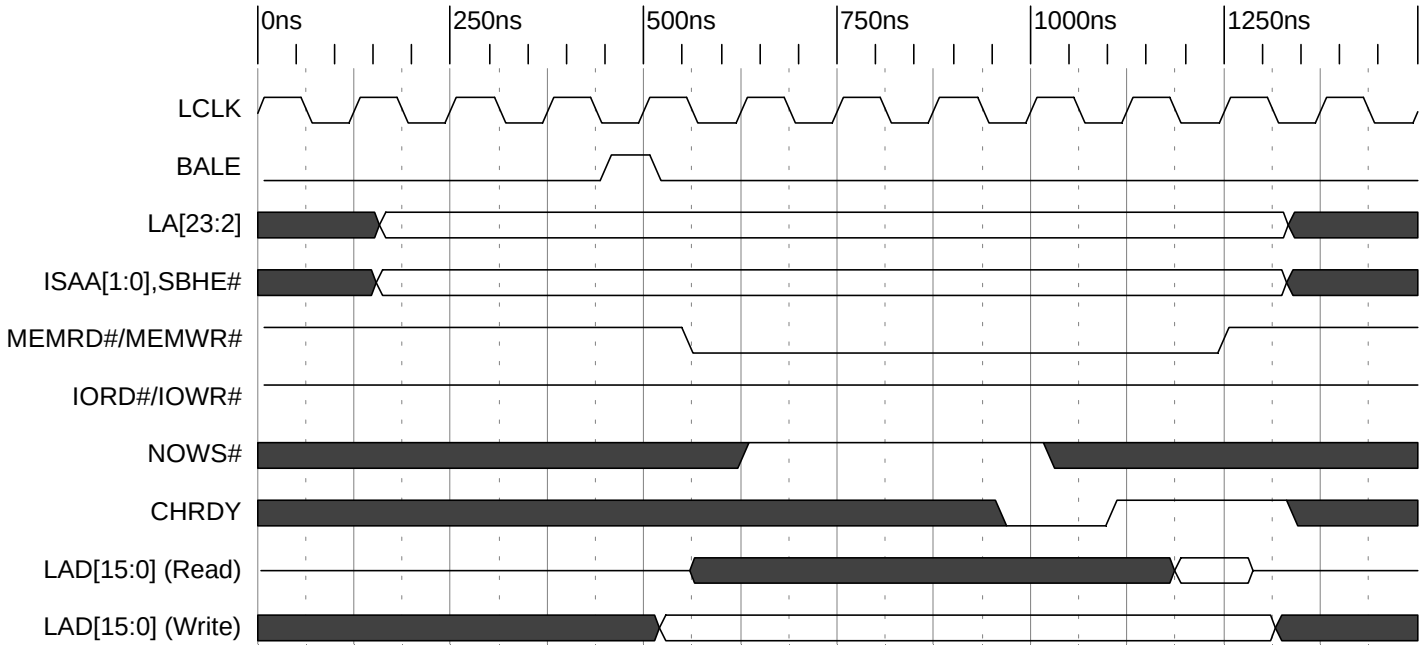
Burst enabled (burst read of four words)
Address-to-data = one wait state
Data-to-data = zero wait states
Read strobe = three wait states

Timing Diagram 9-36. Direct Slave Burst Read and Multiplexed Local Bus (16-Bit Local Bus, J Mode)

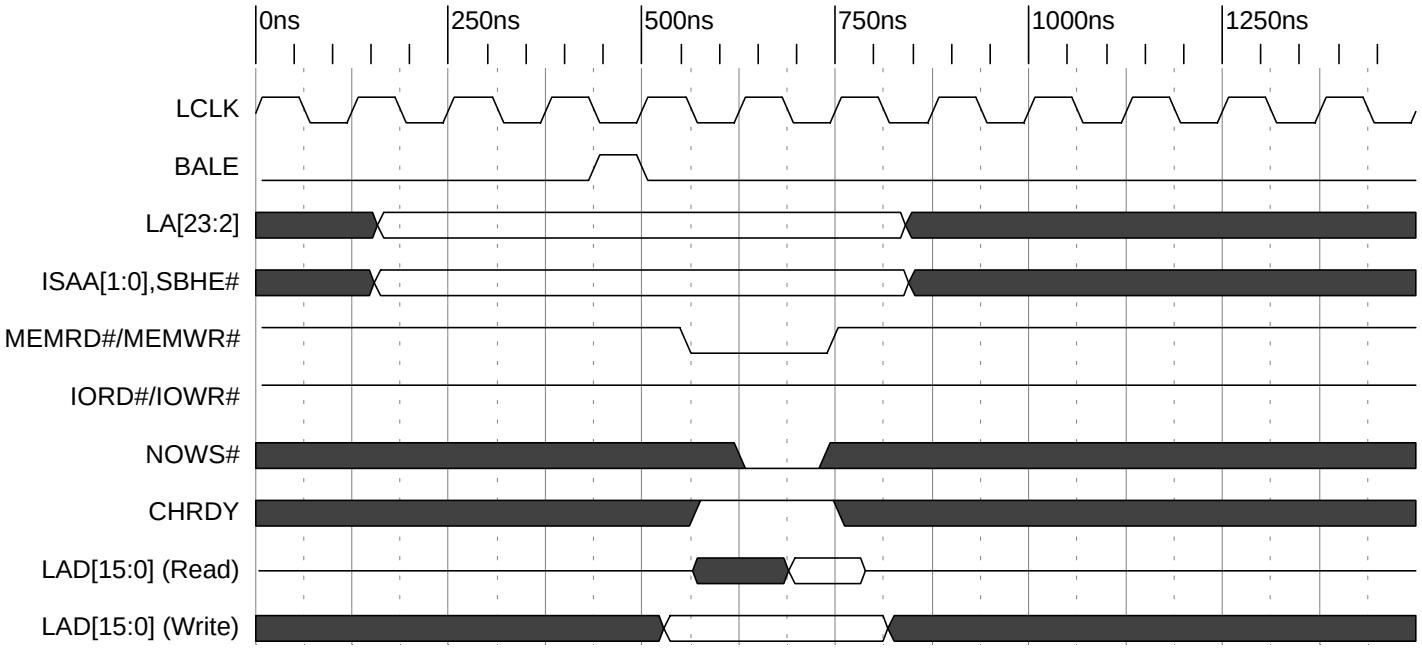
9.2 ISA Timing Diagrams



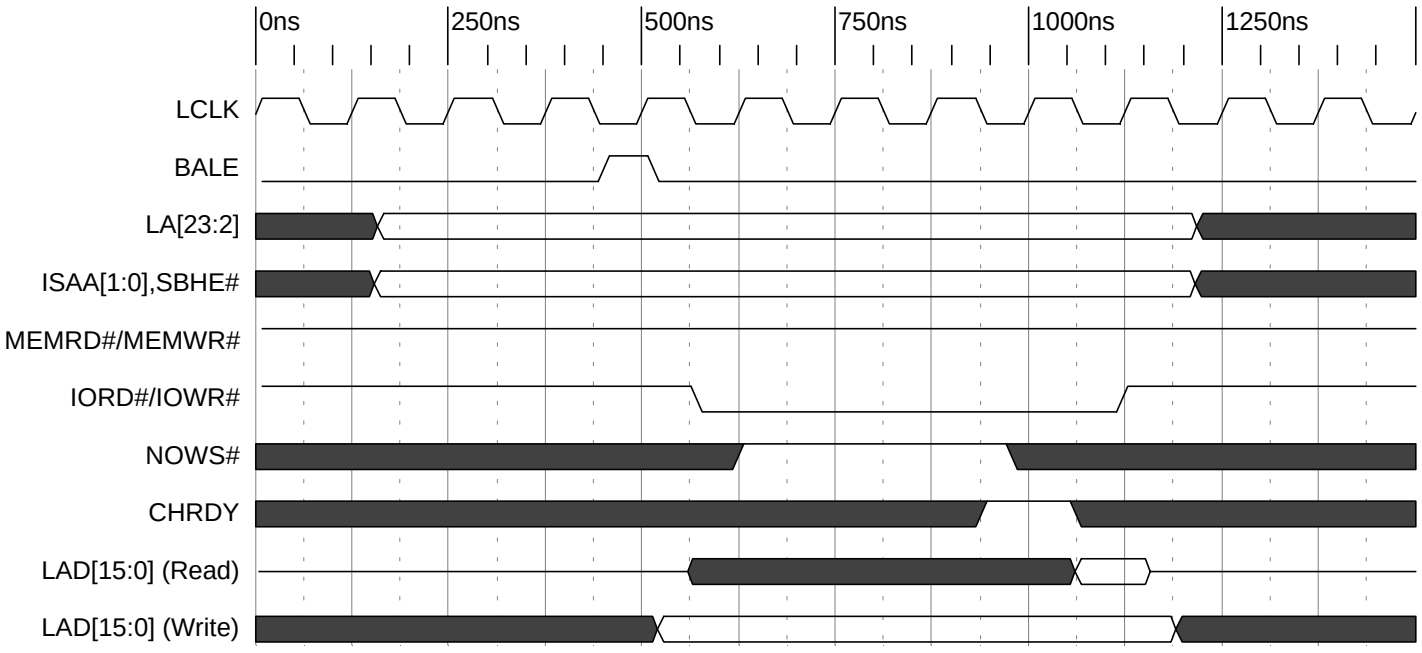
Timing Diagram 9-37. 8-Bit Memory Read/Write Standard ISA Cycle (6 LCLK Shown)



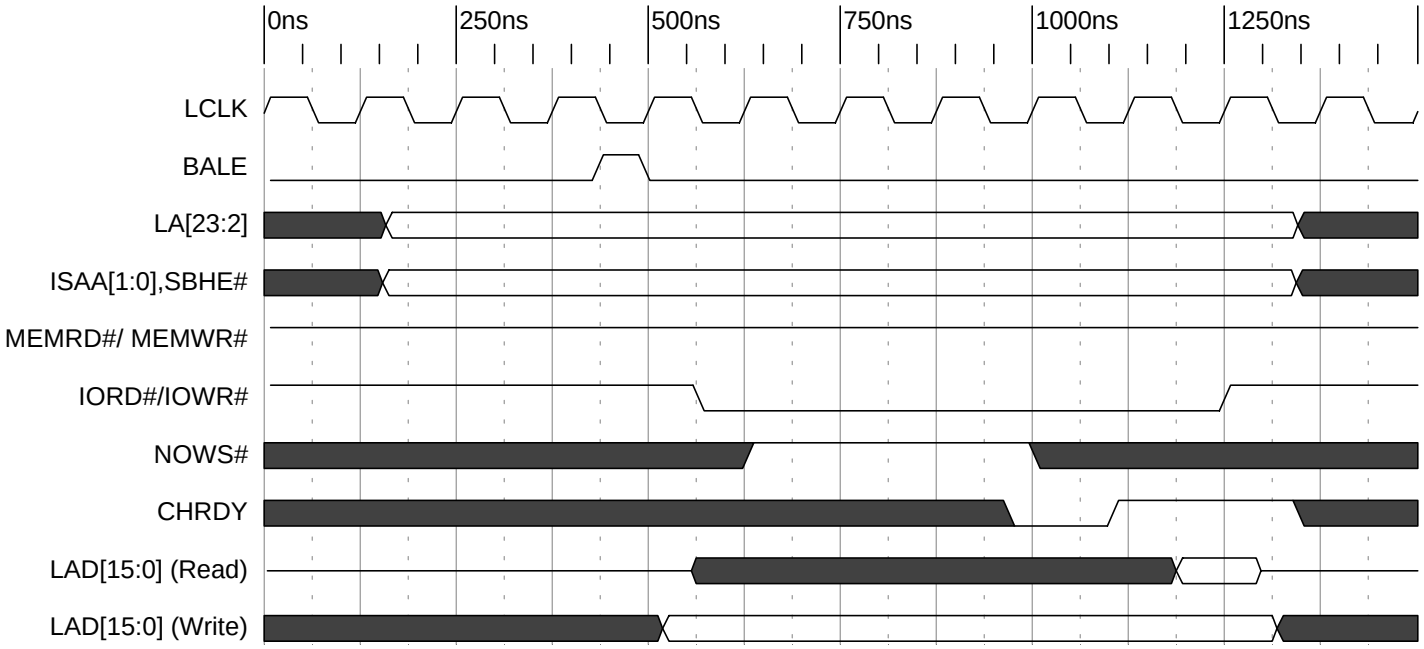
Timing Diagram 9-38. 8-Bit Memory Read/Write Extended ISA Cycle (7 LCLK Shown)



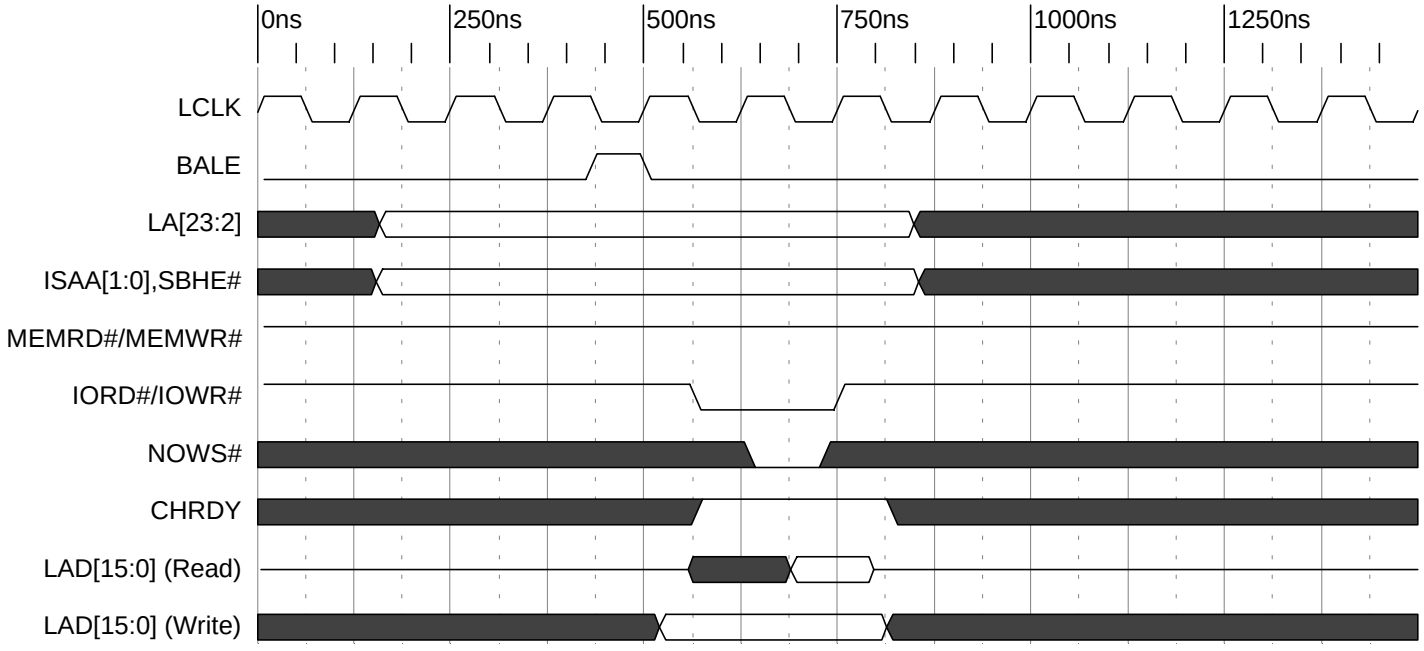
Timing Diagram 9-39. 8-Bit Memory Read/Write Compressed ISA Cycle (3 LCLK Shown)



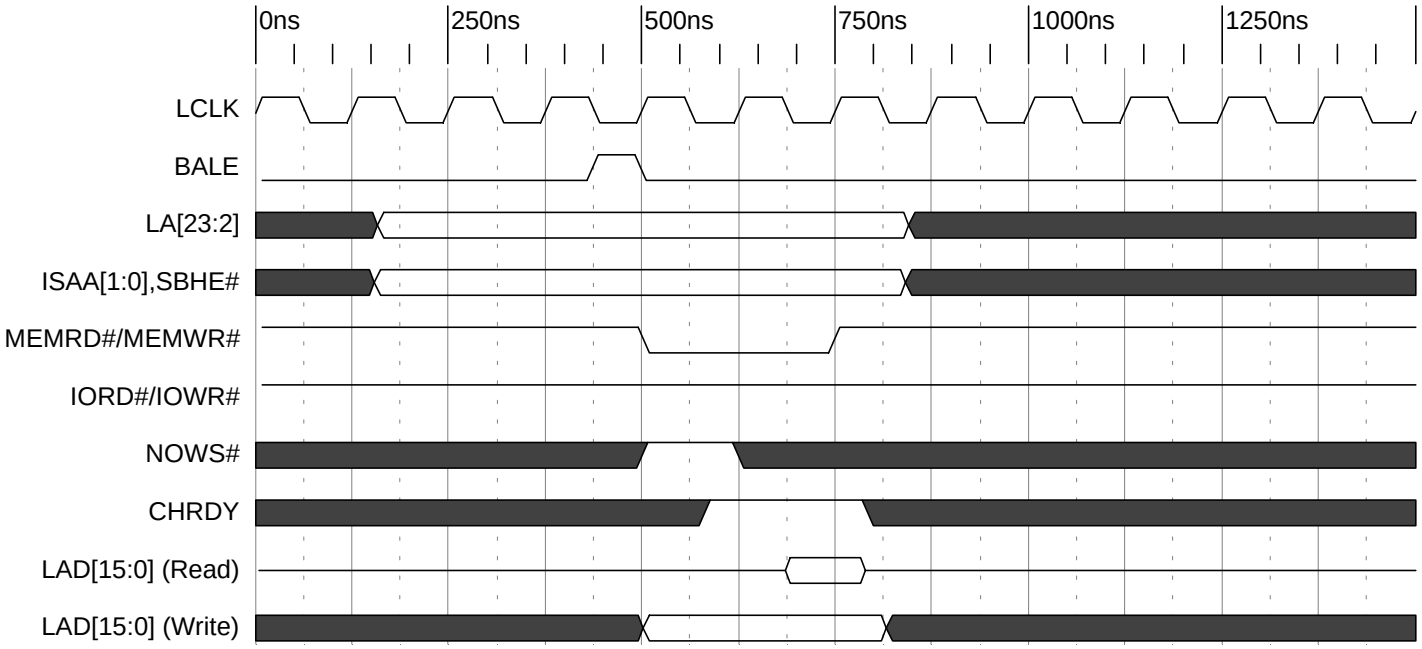
Timing Diagram 9-40. 8-Bit I/O Read/Write Standard ISA Cycle (6 LCLK Shown)



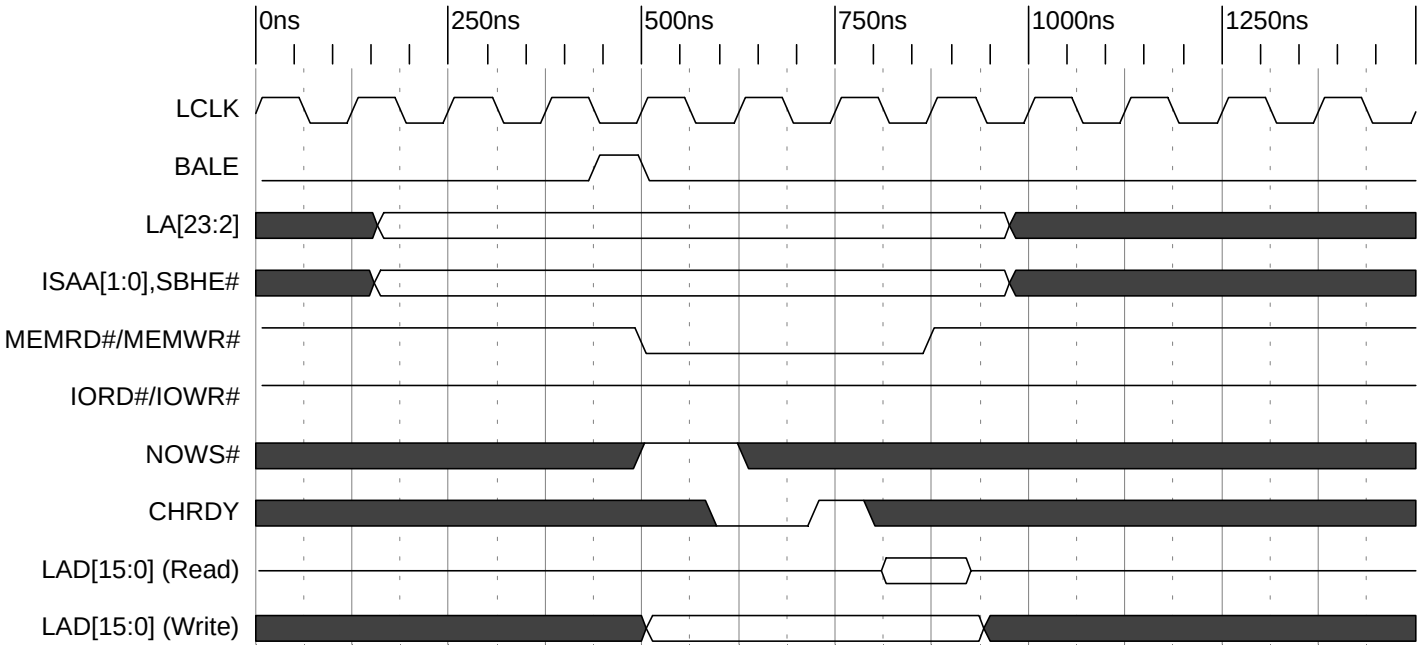
Timing Diagram 9-41. 8-Bit I/O Read/Write Extended ISA Cycle (7 LCLK Shown)



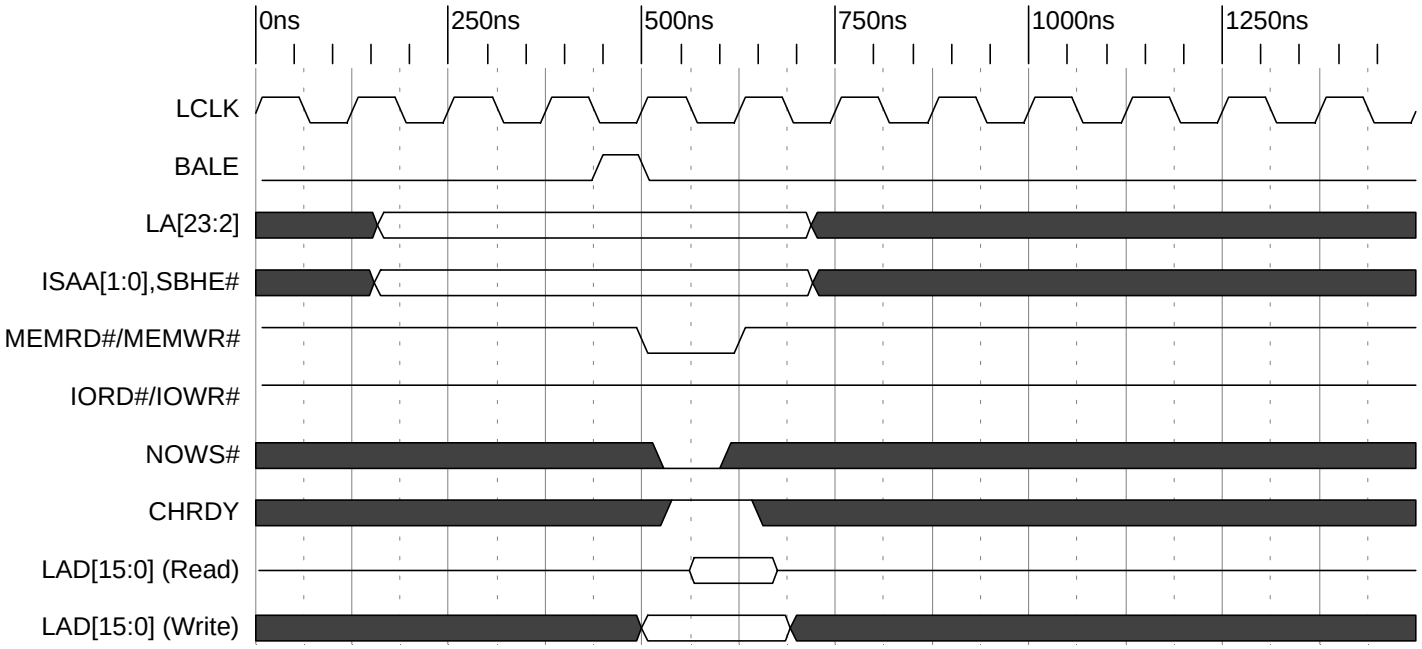
Timing Diagram 9-42. 8-Bit I/O Read/Write Compressed ISA Cycle (3 LCLK Shown)



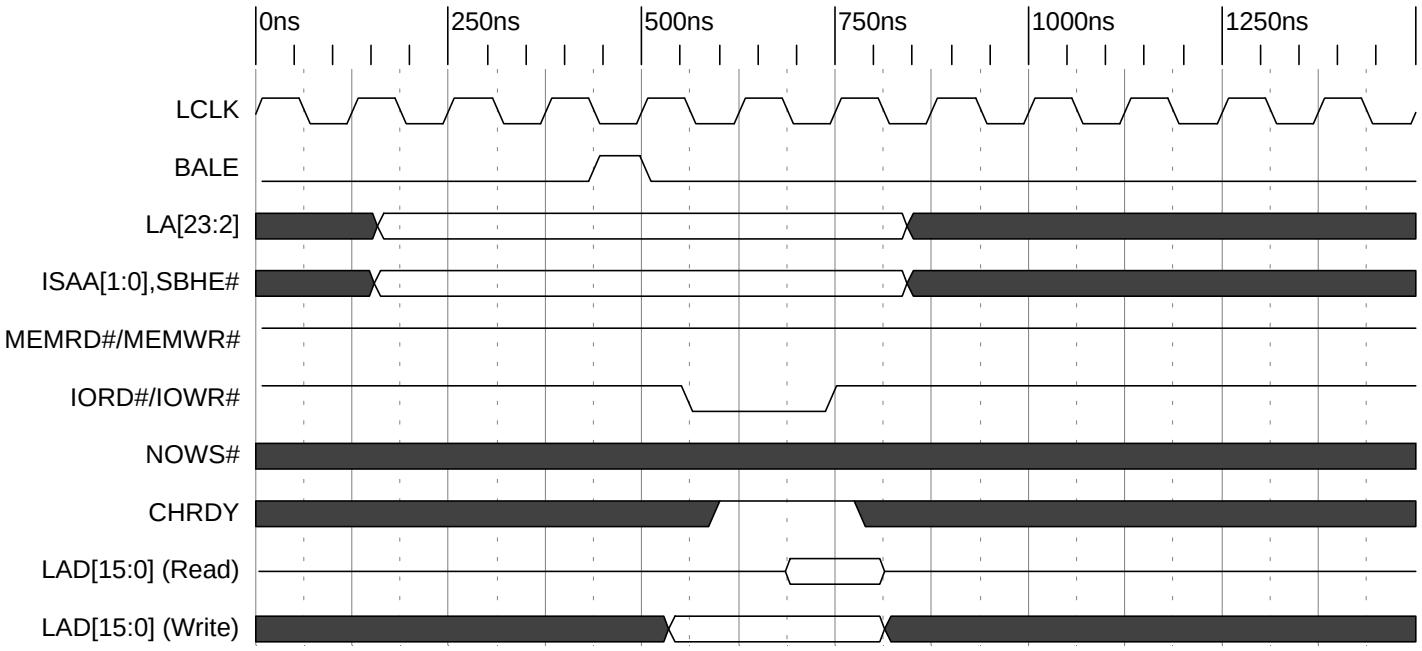
Timing Diagram 9-43. 16-Bit Memory Read/Write Standard ISA Cycle (3 LCLK Shown)



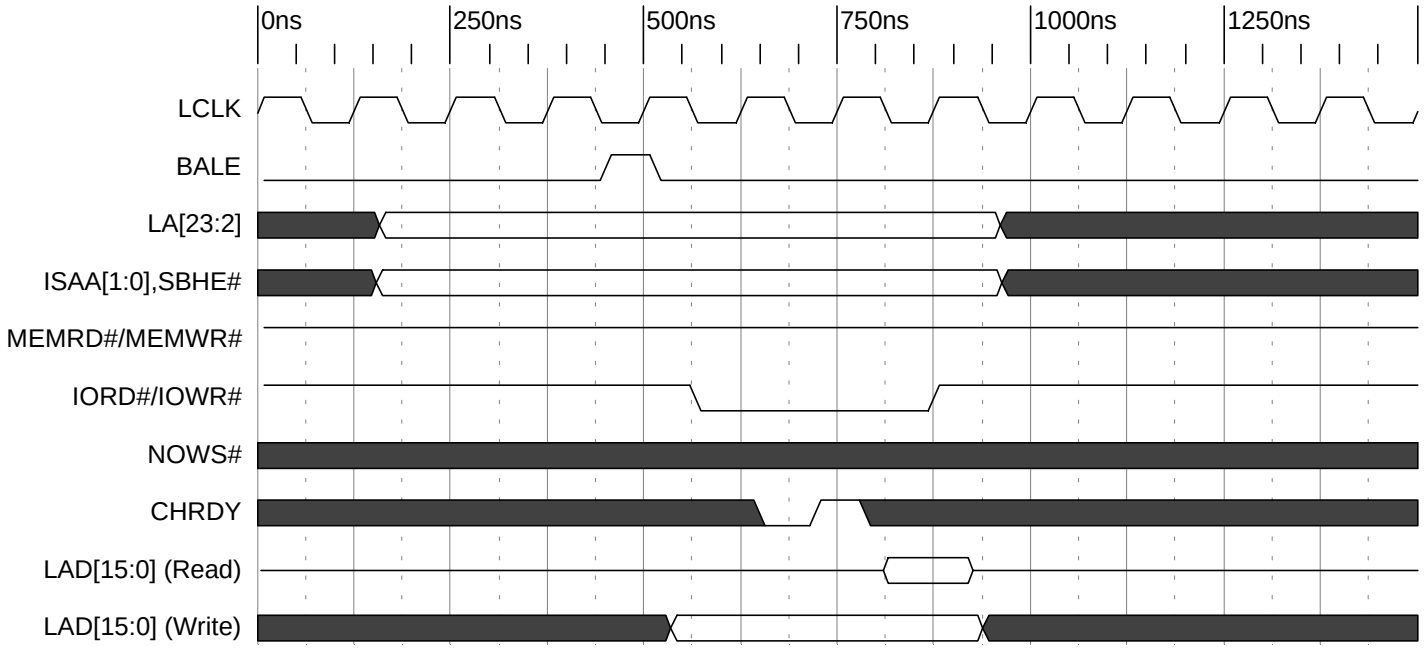
Timing Diagram 9-44. 16-Bit Memory Read/Write Extended ISA Cycle (4 LCLK Shown)



Timing Diagram 9-45. 16-Bit Memory Read/Write Compressed ISA Cycle (2 LCLK Shown)



Timing Diagram 9-46. 16-Bit I/O Read/Write Standard ISA Cycle (3 LCLK Shown)



Timing Diagram 9-47. 16-Bit I/O Read/Write Extended ISA Cycle (4 LCLK Shown)