

\*\*\* RTX-02A 8255 I/O CARD \*\*\*

1. INTRODUCTION

THE RTX-02A 8255 I/O CARD IS A PROGRAMABLE INPUT/OUTPUT INTERFACE FOR IBM PC/XT/AT, 386, 486 OR COMPATIBLE COMPUTER. IT CONTAINS 72 I/O LINE, 3 INDEPENDENT 16 BIT COUNTERS, EACH WITH A COUNT RATE OF UP TO 2MHz. ALL MODES OF OPERATION ARE SOFTWARE PROGRAMABLE. THE BOARD'S BASE I/O ADDRESS IS JUMPER SELECTABLE TO ONE OF SIXTEEN I/O LOCATION. ALL EXTERNAL I/O WITH THE RTX-02A IS DONE THROUGH 40-PINS AND 26-PINS PIN HEADERS. THAT IS ACCESSIBLE THROUGH THE REAR PANEL OF THE COMPUTER AFTER THE BOARD IS INSTALLED.

2. FEATURES

- \* 3 STANDARD PPI DIGITAL CONTROLLERS. ( ONE OPTIONAL )
- \* 3 INDEPENDENT 16 BIT COUNTER.
- \* INTERNAL/EXTERNAL CLOCK SELECT BY JUMPER.
- \* 2 INTERNAL CLOCK SELECT BY JUMPER.
- \* BASE ADDRESS UP TO SIXTEEN SETS.

&H200 - &H20F.	&H210 - &H21F.	&H240 - &H24F.	&H250 - &H25F.
&H280 - &H28F.	&H290 - &H29F.	&H2C0 - &H2CF.	&H2D0 - &H2DF.
&H300 - &H30F.	&H310 - &H31F.	&H340 - &H34F.	&H350 - &H35F.
&H380 - &H38F.	&H390 - &H39F.	&H3C0 - &H3CF.	&H3D0 - &H3DF.

- \* CLEAR PIN'S SIGNAL ON BOARD.
- \* 24 LEDS DISPLAY FOR EACH PPI PORT A.
- \* ALL PORTS CAN BE ENABLE/DISABLE.

3. INSTALLATION

THE RTX-02A PLUGS INTO ANY EXPANSION SLOT, INCLUDING A SHORT SLOT, OF AN IBM PC/XT/AT, 386, 486, 586 OR COMPATIBLE COMPUTER. IT MAY BE ADVANTAGEOUS, THEREFORE, TO CHOOSE AN AVAILABLE SHORT SLOT INSIDE THE COMPUTER. THE BOARD'S I/O BASE IS JUMPER SELECTABLE; PREVENTING POSSIBLE CONTENTION WITH OTHER DEVICES SIMPLY INVOLVES CHANGING THIS JUMPER. IF THE BOARD ADDRESS IS UNJUMPED OR INCORRECT, THE RTX-02A WILL NOT OPERATE. THE PIN HEADERS PROVIDES FOR A VARIETY OF I/O CONNECTIONS TO BE MADE TO THE PROGRAMMABLE INTERVAL TIMER (PIT). EACH OF THE COUNTER INPUT MAY BE JUMPED TO EITHER INTERNAL CLOCK OR AN EXTERNAL CLOCK INPUT.

3.1 JUMPER SETTINGS

BASE ADDRESS SELECTION - JP1, JP2

TO SELECT THE BOARD'S BASE I/O ADDRESS, THE JUMPER ON THE CONNECTOR LABELED JP1 MUST BE POSITIONED TO CORRESPOND TO THE ADDRESS DESIRED. THE JUMPER SHOULD BE PLACED VERTICALLY ACROSS THE PAIR OF HEADER PINS BELOW THE BASE ADDRESS SELECTED. THE BASE ADDRESSES LABELED ABOVE CONNECTOR JP1 ARE HEXADECIMAL VALUES.

THE RTX-02A BASE ADDRESS IS PRESET TO X"200". IF THE BASE ADDRESS IS CHANGED FROM THE PRESET VALUE. THE EXAMPLE SOFTWARE PROVIDED WITH THE RTX-02A WILL NEED TO BE MODIFIED TO REFLECT THE NEW VALUE.

JP2	JP1	BASE ADDRESS
X X X X 0 0 0 0 X X X X 0 0 0 0	X 0 0 0 0 0 0 0 X 0 0 0 0 0 0 0	200
0 0 0 0 X X X X 0 0 0 0 X X X X	X 0 0 0 0 0 0 0 X 0 0 0 0 0 0 0	210
X X X X 0 0 0 0 X X X X 0 0 0 0	0 X 0 0 0 0 0 0 0 X 0 0 0 0 0 0	240
0 0 0 0 X X X X 0 0 0 0 X X X X	0 X 0 0 0 0 0 0 0 X 0 0 0 0 0 0	250
X X X X 0 0 0 0 X X X X 0 0 0 0	0 0 X 0 0 0 0 0 0 0 X 0 0 0 0 0	280
0 0 0 0 X X X X 0 0 0 0 X X X X	0 0 X 0 0 0 0 0 0 0 X 0 0 0 0 0	290
X X X X 0 0 0 0 X X X X 0 0 0 0	0 0 0 X 0 0 0 0 0 0 0 X 0 0 0 0	2C0
0 0 0 0 X X X X 0 0 0 0 X X X X	0 0 0 X 0 0 0 0 0 0 0 X 0 0 0 0	2D0
X X X X 0 0 0 0 X X X X 0 0 0 0	0 0 0 0 X 0 0 0 0 0 0 0 X 0 0 0	300
0 0 0 0 X X X X 0 0 0 0 X X X X	0 0 0 0 X 0 0 0 0 0 0 0 X 0 0 0	310
X X X X 0 0 0 0 X X X X 0 0 0 0	0 0 0 0 0 X 0 0 0 0 0 0 0 X 0 0	340
0 0 0 0 X X X X 0 0 0 0 X X X X	0 0 0 0 0 X 0 0 0 0 0 0 0 X 0 0	350
X X X X 0 0 0 0 X X X X 0 0 0 0	0 0 0 0 0 0 X 0 0 0 0 0 0 0 X 0	380
0 0 0 0 X X X X 0 0 0 0 X X X X	0 0 0 0 0 0 X 0 0 0 0 0 0 0 X 0	390
X X X X 0 0 0 0 X X X X 0 0 0 0	0 0 0 0 0 0 0 X 0 0 0 0 0 0 0 X	3C0
0 0 0 0 X X X X 0 0 0 0 X X X X	0 0 0 0 0 0 0 X 0 0 0 0 0 0 0 X	3D0

### 3.2 RTX-02A SYSTEM BOARD DEFAULT

&H200 - &H20F

&H200 --- PORT1 A READ WRITE BUFFER  
&H201 --- PORT1 B READ WRITE BUFFER  
&H202 --- PORT1 C READ WRITE BUFFER  
&H203 --- 8255 (U1) CONTROL REGISTER  
&H204 --- PORT2 A READ WRITE BUFFER  
&H205 --- PORT2 B READ WRITE BUFFER  
&H206 --- PORT2 C READ WRITE BUFFER  
&H207 --- 8255 (U2) CONTROL REGISTER  
&H208 --- PORT3 A READ WRITE BUFFER  
&H209 --- PORT3 B READ WRITE BUFFER  
&H20A --- PORT3 C READ WRITE BUFFER  
&H20B --- 8255 (U3) CONTROL REGISTER  
&H20C --- COUNTER 0 READ WRITE BUFFER  
&H20D --- COUNTER 1 READ WRITE BUFFER  
&H20E --- COUNTER 2 READ WRITE BUFFER  
&H20F --- COUNTER CHIP 8253 CONTROL REGISTER

### 3.3 RTX-02A INTERNAL/EXTERNAL CLOCK --- JP3

JP3 CAN BE SELECTED INTERNAL OR EXTERNAL CLOCK TO 8253 COUNTER 0, 1, 2. WHEN JUMPER IS SHORT, IT MEANS THE COUNTER USE INTERNAL CLOCK. ELSE USE EXTERNAL CLOCK. NORMAL SETTING IS SHORTED FOR INTERNAL CLOCK INPUT. THE INTERNAL CLOCK IS DESIRED BY THE MOTHER BOARD CLOCK (SLOT B20 -- CLK, SLOT B30 -- OSC). FOR EXAMPLE AS FOLLOW:

PC/XT (B20) --- CLK(4.77MHz) / 2 = 2.385MHz  
PC/AT (B20) --- CLK(8.00MHz) / 2 = 4.000MHz  
PC/AT (B20) --- CLK(10.0MHz) / 2 = 5.000MHz  
PC (B30) --- CLK(14.318MHz) / 2 = 7.159MHz

JP3     x x x  
          x x x     ----- 8253 CLOCK 0 (SHORT FOR INTERNAL CLOCK)  
          \ \     ----- 8253 CLOCK 1 (SHORT FOR INTERNAL CLOCK)  
          \     ----- 8253 CLOCK 2 (SHORT FOR INTERNAL CLOCK)

### 3.4 RTX-02A INTERNAL CLOCK SELECT --- JP4

JP4 CAN BE SELECTED USE THE MOTHER BOARD SIGNAL (B30-OSC, B20-CLK) INPUT. FOR EXAMPLE AS FOLLOW:

JP4     x x o     --- USE SLOT B30 SIGNAL (OSC)  
JP4     o x x     --- USE SLOT B20 SIGNAL (CLK). DEFAULT

#### 4. DEMO PROGRAM LIST

```
100 REM * THE RTX-02A 8255 I/O CARD DEMO PROGRAM *
110 SCREEN 0,0,0 : WIDTH 80,25 : KEY OFF : CLS
120 LOCATE 10,10 : PRINT " THE RTX-02A 8255 I/O CARD DEMO PROGRAM "
130 LOCATE 12,10 : PRINT " THE 8255 PORT A, B, C OUTPUT SQUARE WAVE
140 LOCATE 14,10 : PRINT " 8253 COUNTER 0 DIVIDE BY 2 ..."
150 LOCATE 16,10 : PRINT " COUNTER 0 DIVIDE BY 50 ..."
160 LOCATE 18,10 : PRINT " COUNTER 0 DIVIDE BY 100 ..."
240 REM * 8253 TESTER *
250 PORT = &H20C
260 OUT PORT + 3, &H36
270 OUT PORT + 3, &H76
280 OUT PORT + 3, &HB6
290 OUT PORT + 0, &H2 : OUT PORT + 0, &H0
300 OUT PORT + 1, &H32 : OUT PORT + 1, &H0
310 OUT PORT + 2, &H64 : OUT PORT + 2, &H0
315 REM * 8255 MODE 0 OUTPUT TESTER *
316 REM 8255-1 TEST
317 REM 8255-1 MODE 0 PORT A, B, C OUTPUT
320 PORT = &H200
325 OUT PORT + 3, &H80
330 A=0 : GOSUB 500
335 FOR K=0 TO 1000 : NEXT K
340 A=&FF : GOSUB 500
341 REM 8255-2 TEST
342 REM 8255-2 MODE 0 PORT A, B, C OUTPUT
345 PORT = PORT + 4
350 OUT PORT + 3, &H80
355 A=0 : GOSUB 500
360 FOR K=0 TO 1000 : NEXT K
365 A=&FF : GOSUB 500
366 REM 8255-3 TEST
367 REM 8255-3 MODE 0 PORT A, B, C OUTPUT
370 PORT = PORT + 4
375 OUT PORT + 3, &H80
380 A=0 : GOSUB 500
385 FOR K=0 TO 1000 : NEXT K
390 A=&FF : GOSUB 500
400 GOTO 320
500 FOR I=0 TO 2
510 OUT PORT +I, A
520 NEXT I
530 RETURN
```

5. I/O CONNECTOR

=====  
CN1 PIN ASSIGNMENTS  
=====

PIN 1	GND	PIN 2	GND
3	1A3	4	GND
5	1A2	6	1A1
7	1A0	8	CLK0
9	OUT0	10	GATE0
11	CLK2	12	OUT2
13	GATE2	14	CLK1
15	GATE1	16	OUT1
17	1A4	18	1A5
19	1A6	20	1A7
21	1C7	22	1C6
23	1C5	24	1C4
25	1C0	26	1C1
27	1C2	28	1B7
29	1C3	30	1B6
31	1B0	32	1B5
33	1B1	34	1B4
35	1B2	36	1B3
37	-5V	38	+5V
39	-12V	40	+12V

=====  
CN2 PIN ASSIGNMENTS  
=====

PIN 1	GND	PIN 2	GND
3	GND	4	GND
5	GND	6	GND
7		8	
9		10	
11		12	
13	2A1	14	2A0
15	2A3	16	2A2
17	2A5	18	2A4
19	2A7	20	2A6
21	2C6	22	2C7
23	2C4	24	2C5
25	2C1	26	2C0
27	2B7	28	2C2
29	2B6	30	2C3
31	2B5	32	2B0
33	2B4	34	2B1
35	2B3	36	2B2
37	-5V	38	+5V
39	-12V	40	+12V

=====  
CN3 PIN ASSIGNMENTS  
=====

PIN 1	3A0	PIN 14	3B5
2	3A1	15	3B6
3	3A2	16	3B7
4	3A3	17	3C0
5	3A4	18	3C1
6	3A5	19	3C2
7	3A6	20	3C3
8	3A7	21	3C4
9	3B0	22	3C5
10	3B1	23	3C6
11	3B2	24	3C7
12	3B3	25	GND
13	3B4	26	GND



**FUNCTIONAL DESCRIPTION**

**General**

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Micro-computer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

**Data Bus Buffer**

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INPUT or OUTPUT CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values

**Read/Write Logic**

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

**$\overline{RD}$  (Read)**

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

**$\overline{WR}$  (Write)**

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

**A0, A1**

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

**$\overline{CS}$  (Chip Select)**

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The  $\overline{CS}$  input has no effect upon the actual operation of the counters.

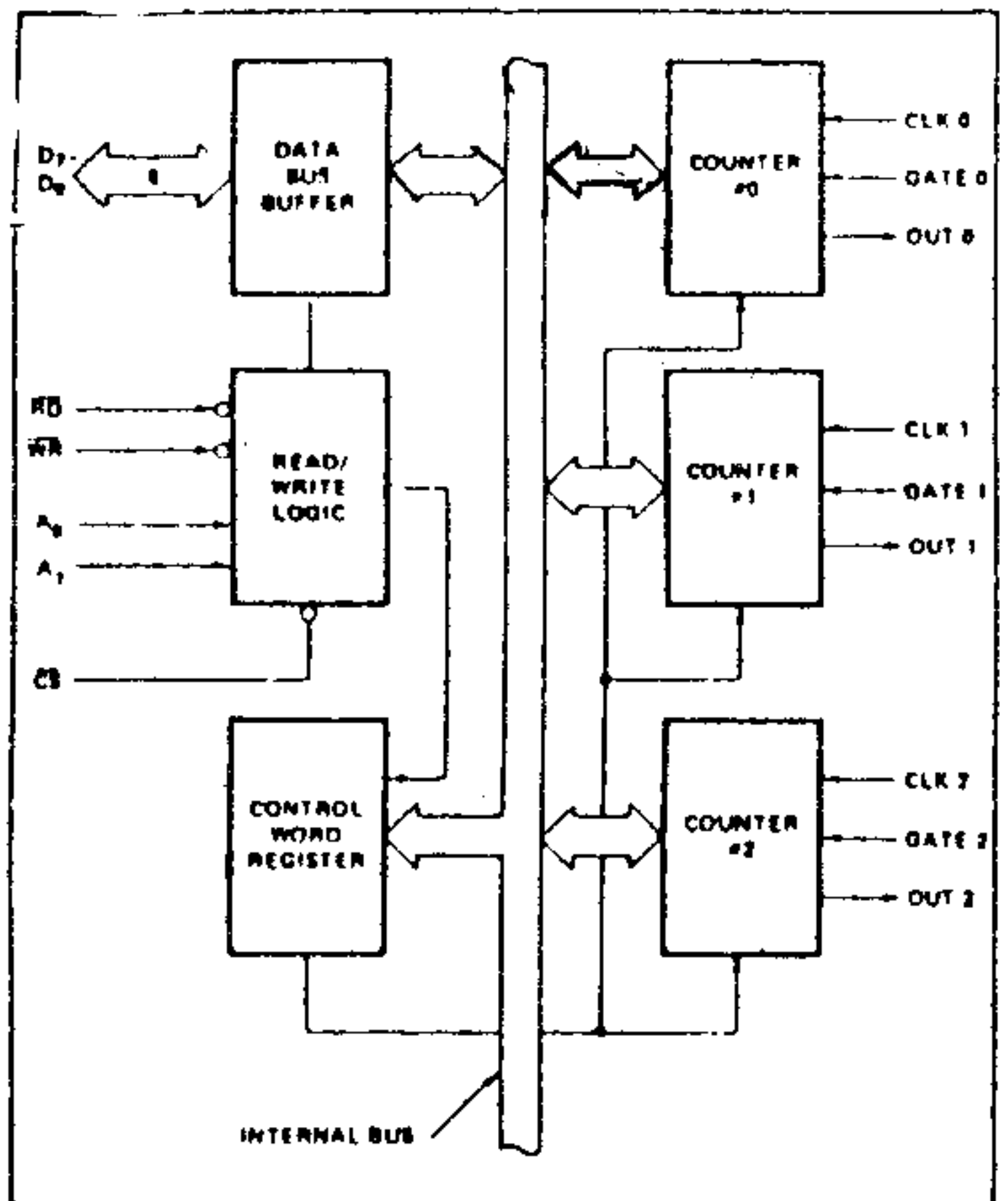


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A <sub>1</sub>	A <sub>0</sub>	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

**Control Word Register**

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

**Counter #0, Counter #1, Counter #2**

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

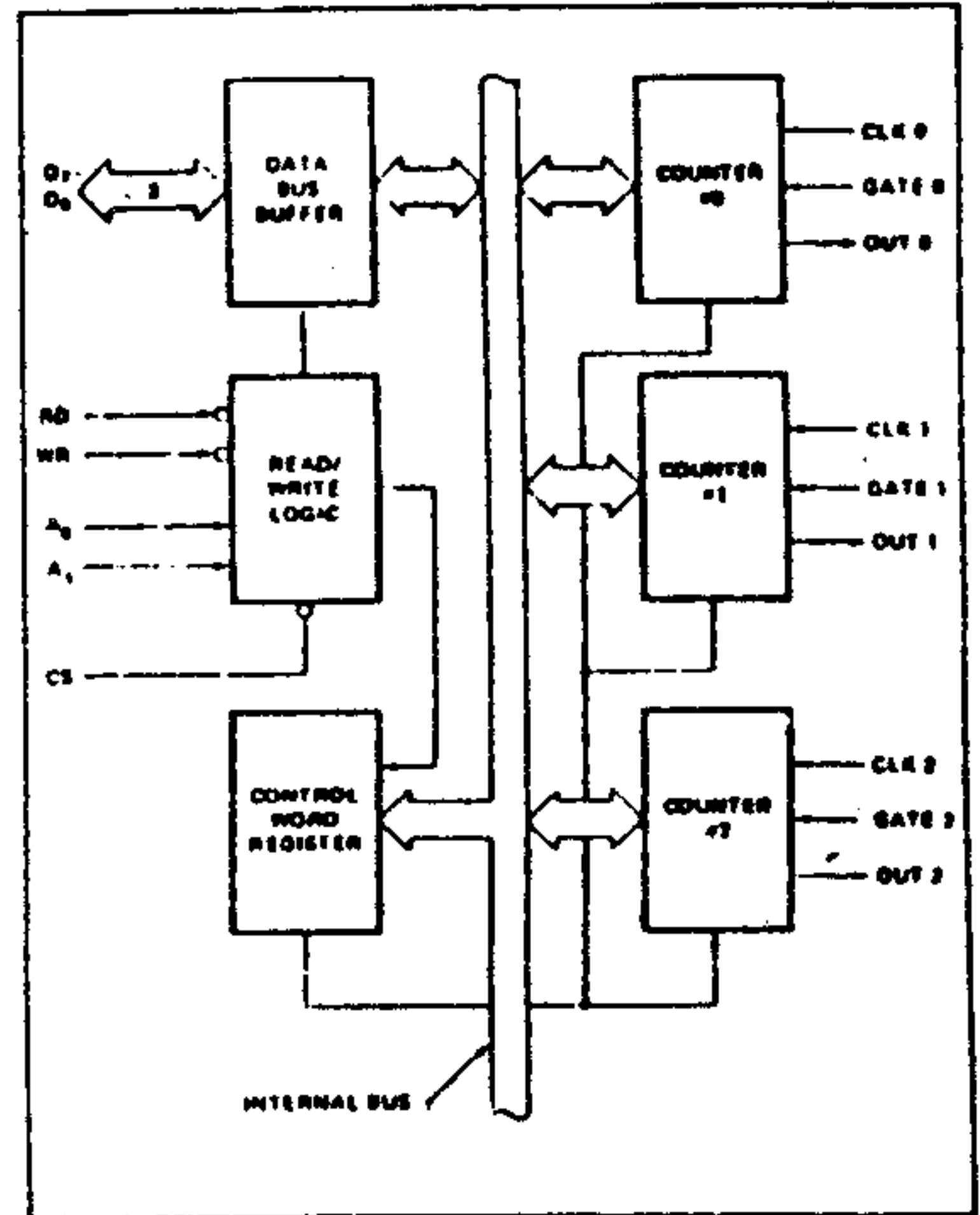


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

**8253 SYSTEM INTERFACE**

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

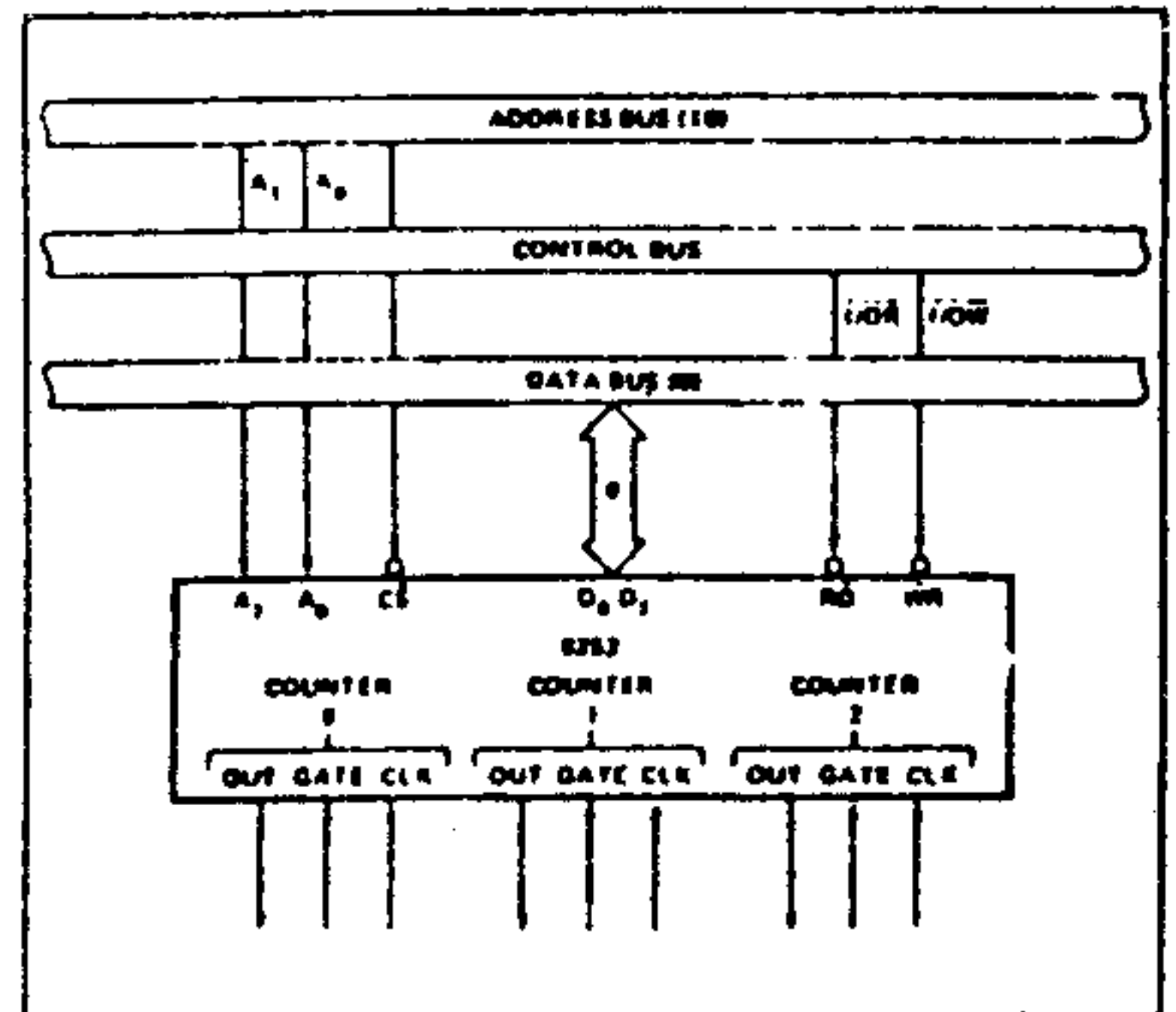


Figure 5. 8253 System Interface

## OPERATIONAL DESCRIPTION

### General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

### Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

### Control Word Format

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

### Definition of Control

#### SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

#### RL — Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

#### M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

#### BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

### Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

### MODE Definition

**MODE 0: Interrupt on Terminal Count.** The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

- (1) Write 1st byte stops the current counting.
- (2) Write 2nd byte starts the new count.

**MODE 1: Programmable One-Shot.** The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

